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Defense Nuclear Agency
Alexandria, VA 22310-3398

DNA-TR-92-58

Research on Radiation Effects in Support of the Defense Nuclear Agency

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January 1993

Technical Report

93-03870
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REPORT DOCUMENTATION PAGE

1. AGENCY USE ONLY (Leave blank)	2. REPORT DATE 930101	3. REPORT TYPE AND DATES COVERED Technical 880229 – 911231

4. TITLE AND SUBTITLE	5. FUNDING NUMBERS
Research on Radiation Effects in Support of the Defense Nuclear Agency	C - DNA 001-88-C-0004 PE - 62715H
6. AUTHOR(S) Kenneth F. Galloway and Ronald D. Schrimpf	PR - RV TA - RA WU - DH032870

7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES)	8. PERFORMING ORGANIZATION REPORT NUMBER
Arizona Board of Regents Electrical & Computer Engineering Dept. University of Arizona Tucson, AZ 85721	

9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES)	10. SPONSORING/MONITORING AGENCY REPORT NUMBER
Defense Nuclear Agency 6801 Telegraph Road Alexandria, VA 22310-3398 RAEE/Palkuti	DNA-TR-92-58

11. SUPPLEMENTARY NOTES

This work was sponsored by the Defense Nuclear Agency under RDT&E RMC Code B4662D RV RA EA00148 RAEE 3260A 25904D.

12a. DISTRIBUTION/AVAILABILITY STATEMENT	12b. DISTRIBUTION CODE
Approved for public release; distribution is unlimited.	

13. ABSTRACT (Maximum 200 words)

Because of their higher switching speeds, power MOSFETs are favored over power BJTs in spaceborne and military applications where size and weight are important. However, power MOSFETs are subject to degradation and failure mechanisms in radiation environments, including single event burnout, reduction of breakdown voltage, threshold shifts, and loss of current drive. This report discusses radiation–effects research in the areas of single event burnout of power MOSFETs and power BJTs, simulation of the effect of ionizing radiation on power–MOSFET breakdown voltage, charge buildup in field oxides, and $1/f$ noise in power MOSFETs. A model for single event burnout is presented and structural changes to reduce susceptibility are provided. A simulation tool for designing high–voltage termination structures is presented and applied to field–ring and field–plate terminations. Guidelines to minimize breakdown–voltage degradation are given. A method of correlating charge buildup in field oxides to that in test devices is discussed. The use of $1/f$ noise as a radiation–effects characterization tool in power MOSFETs is examined. This work is intended to: (1) facilitate selection of appropriate power MOSFETs for radiation environments and (2) provide design techniques to improve the radiation hardness of power MOSFETs.

14. SUBJECT TERMS			15. NUMBER OF PAGES 126
Power MOSFETs	Radiation Effects	$1/f$ Noise in MOSFETs	
Single Event Burnout	Simulation of Power MOSFETs	Breakdown Voltage	16. PRICE CODE

17. SECURITY CLASSIFICATION OF REPORT	18. SECURITY CLASSIFICATION OF THIS PAGE	19. SECURITY CLASSIFICATION OF ABSTRACT	20. LIMITATION OF ABSTRACT
UNCLASSIFIED	UNCLASSIFIED	UNCLASSIFIED	SAR

CLASSIFIED BY:

N/A since Unclassified.

DECLASSIFY ON:

N/A since Unclassified.

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I. Introduction and Executive Summary

This final report describes work for Contract No. DNA001-88-C-0004. The start date for this effort was 29 February 1988.

The two original technical thrusts of this project were: (1) Modeling of Single Event Burnout in Power MOSFETs and (2) Simulation of the Effect of Ionizing Radiation on Power MOSFET Breakdown Voltage. In addition, work was added in the following areas: (3) Single Event Burnout of Power Bipolar Transistors; (4) Charge Buildup in Field Oxides; and (5) $1/f$ Noise Measurements in Power MOSFETs.

Heavy ions, ubiquitous in a space environment, can cause single event burnout (SEB) in power MOSFETs. This is a catastrophic failure mechanism that is initiated by the passage of a heavy ion through the device structure. This event generates a current filament that locally turns on a parasitic npn transistor inherent to the power MOSFET physical structure. Subsequent high currents and high voltage in the power MOSFET induce second breakdown of the parasitic transistor and meltdown of the power MOSFET. During the course of the work described in this final report, a model was developed to describe the burnout mechanism and to predict the SEB threshold in terms of linear energy transfer (LET) of the incident heavy ion for a specified device structure and operating condition. This is discussed in Section II.

In addition, the formalisms developed were used to explain single event burnout observed in power bipolar transistors. This work is presented in Section III. The paper "Single-Event Burnout of Power Bipolar Junction Transistors" authored by Jeffrey L. Titus, Gregory H. Johnson, Ronald D. Schrimpf, and Kenneth F. Galloway won the Outstanding Conference Paper Award for the 1991 NSREC in San Diego (the paper is included as Section III.B). This paper presents experimental evidence that power bipolar junction transistors are susceptible to catastrophic failure in a cosmic ray environment. Several types of commercially available power transistors were characterized using the tandem Van de Graaff accelerator at Brookhaven National Laboratory. Most device types that were exposed to a mono-energetic ion with an LET greater than 27 $MeV\text{-}cm^2/mg$ exhibited burnout at collector-emitter voltages less than their rated breakdown voltage. Failure analysis performed on burned out devices indicates that the failure mechanism is similar to thermal runaway induced by second breakdown. A semi-analytical model was developed based on the work on burnout of power MOSFETs to explain this failure mechanism. The model suggests a strong correlation between single-event burnout susceptibility and key layout and processing parameters. The experimental results dictate that system designers should seriously consider the impact of single-event burnout of

power bipolar transistors in space applications.

Another segment of this work was devoted to developing a tool for simulating the performance of power-MOSFET termination structures in ionizing radiation environments. This effort is covered in Section IV. The simulation code that was developed is entitled ASEPS (Arizona SEmiconductor Power device Simulator). ASEPS is a two-dimensional code that solves Poisson's equation for reverse-biased junctions, using the assumption that there is no current flowing in the device. The advantages of ASEPS are short simulation times compared to general purpose device simulation tools and simple inclusion of radiation-induced charge densities. The simulations always converge, independent of such parameters as grid spacing and biasing vol^t ... Typical simulation times on a 386-based machine with coprocessor are one minut. .r simple structures, and three minutes for more complex structures. A PC-based version of the ASEPS code has been completed and is available to DNA contractors.

Work on simulating the effects of ionizing radiation on power MOSFET breakdown voltage lead to the problem of correlating the radiation-induced charge to the total dose in power device termination structures. The solution of this problem is given in Section V.

The paper "Predicting Worst-Case Charge Buildup in Power-Device Field Oxides" by Kosier et al. (included as Section V.B) makes the link, for the first time, between charge buildup in field oxides of test structures (such as MOS capacitors and lateral MOSFETs) and charge buildup in field oxides of power devices. This information is critical for designing radiation-tolerant power devices. Previous work has focused on minimizing sensitivity to oxide charge with no regard as to how much charge can realistically be expected in the structure. This work provides a closed-form worst-case expression for how much charge will accumulate in the power device field oxide. This expression is suitable for design purposes.

Previously, continuous and uniform buildup of oxide charge with total ionizing dose was assumed to occur in every termination structure. This work allows prediction of the charge-saturation effects that are seen in actual device structures. Devices can now be designed to accumulate only as much charge as desired. Previously, charge buildup was modeled as being uniform with lateral position; now, the reality of nonuniform charge buildup has been shown and a method to simulate it has been provided. The models rely on the field-collapse model of charge buildup in the oxide; however, the methods described in the paper will work for any other relationship between charge buildup and electric field in the oxide. The methods and procedures are simple and predictive. They can be applied immediately to radiation-hardened power device designs. ASEPS played

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an important role in establishing the link between experimental breakdown-voltage degradation data and charge buildup in the field oxide. The devices tested in the work were DMOS devices developed at AT&T Bell Labs as part of the Rad-Hard PIC Development program.

Section VI covers work on the effects of ionizing radiation on $1/f$ noise in power MOSFETs. The term "$1/f$ noise" is used generically to refer to all noise that is described by an equation of the form:

$$S(f) = \frac{A}{f^{\lambda}} \qquad (1)$$

where f is the frequency, $S(f)$ is the noise spectrum, and A and λ are constants.

n-channel and p-channel power MOSFETs were exposed to ionizing radiation in a Co-60 source. The interface-trap density was compared to the noise spectrum at each measurement point to establish the relationships among noise voltage, bias conditions, and interface-trap density. In addition the relationship between pre-irradiation noise and charge buildup was examined. The devices were characterized using the subthreshold-slope technique in addition to $1/f$ noise measurements to allow comparison between the noise properties and the radiation-induced charge densities.

The experiments examined the variation of both A and λ from Eq. (1) with total dose. For all devices tested, the magnitude of the noise increased with total dose. For devices biased in the saturation region, the slope (λ) changed with total dose, approaching unity. Although it is more difficult to bias power MOSFET in the linear region, this bias condition yielded $1/f$-noise measurements that are more reliable than those made in the saturation region. The noise behavior of p- and n-channel devices biased in the linear region was compared and contrasted. While the noise magnitude in n-channel devices correlated well with oxide trapped charge, in p-channel devices the correlation was actually better with interface trapped charge.

The following sections greatly expand on the items briefly introduced in this Introduction and Executive Summary. Section II covers Modeling of Single Event Burnout of Power MOSFETs, Section III describes the extension to Single Event Burnout of Power Bipolar Transistors, and Section IV covers Simulation of the Effect of Ionizing Radiation on Power-MOSFET Breakdown Voltage. Sections V and VI discuss work on Charge Buildup in Field Oxides and $1/f$ Noise in Power MOSFETs, respectively. The Summary and Conclusions are in Section VII and Section VIII contains Acknowledgments.

II. Modeling of Single Event Burnout of Power MOSFETs

II.A   Introduction

Single event burnout of double-diffused MOS (DMOS) power transistors occurs due to turn-on of the parasitic bipolar transistor in the DMOS structure by a heavy ion. As part of this task, a model for single event burnout was developed that offers a clear picture of the relationships between the device structural parameters and the properties of the ion-induced current filament. This will allow production of power MOSFETs with decreased susceptibility to single event burnout.

The parasitic bipolar transistor is formed by the n^+ source (emitter), the p body (base) and the n drain (collector). When a heavy ion passes through the device, it generates a filament of charge along its path. The electrons in the filament are transported to the drain terminal by the electric field, while the holes move toward the p body. Before the holes can be removed from the device, they must flow laterally through the parasitic resistance of the body region. The source and body regions are shorted together at the surface of the device by the source metallization, preventing turn-on of the parasitic bipolar transistor in normal device operation. However, the resistive voltage drop generated by the returning holes is of the polarity required to forward bias the emitter junction of the parasitic BJT.

When the emitter of the parasitic BJT is forward biased, electrons are injected into the base and collected by the reverse-biased drain-body (collector) junction. These electrons undergo avalanche multiplication in the drain-body depletion region, generating additional holes that must flow through the parasitic body resistance to ground. If enough holes are generated, the process becomes self-sustaining, the drain current locally increases to a very high level, and the device burns out. The parasitic resistance of the body region is extremely important in determining the critical ion LET (linear energy transfer) at which the device will burnout. The parasitic resistance can be reduced by extending a "p^+ plug" from the body contact toward the channel region of the power MOSFET.

The process by which the parasitic bipolar transistor turns on is controlled by avalanche generation of carriers in the drain-body depletion region and the voltage drop developed along the body region by the return of the avalanche-generated holes to ground. A feedback model that describes this process was developed under this contract and described in detail in several technical publications. The papers describing the model are included in Sections II.B–II.E. This collection of papers represents the most comprehensive description of the single-event burnout process that has been prepared to

date. A brief overview of each paper is included here to guide the reader through this material.

Section II.B: G.H. Johnson, J.H. Hohl, R.D. Schrimpf, and K.F. Galloway, "Simulating Single-Event Burnout of N-Channel Power MOSFETs," *IEEE Trans. Electron Devices*, submitted for publication, 1992.

This paper presents the most complete description of the model. It begins with an overall discussion of the burnout process and the heavy-ion-induced current filament. A model is presented for the parasitic-BJT operation, including the feedback mechanism, generation of holes due to avalanching, and the turn-on time of the device following an ion strike. Finally, some typical burnout thresholds are calculated and the critical LET for burnout is plotted vs. the extent of the p^+ plug.

Section II.C: J.H. Hohl and K.F. Galloway, "Analytical Model for Single Event Burnout of Power MOSFETs," *IEEE Trans. Nucl. Sci.*, vol. NS-34, pp. 1275-1280, 1987.

This paper introduces the method of calculating the number of holes returning due to avalanching in the drain-body depletion region. It also calculates the initial forward bias that appears on the parasitic emitter junction using an electrostatic solution based on the method of images.

Section II.D: J.H. Hohl and G.H. Johnson, "Features of the Triggering Mechanism for Single Event Burnout of Power MOSFETs," *IEEE Trans. Nucl. Sci.*, vol. NS-36, pp. 2260-2266, 1989.

The avalanching conditions in the drain-body depletion region are investigated over a wide range of collector current densities. It is shown that with increasing collector current, the avalanche multiplication factor rises to a peak, declines to a valley, and then monotonically increases. This may lead to the existence of a stable avalanching condition with a collector current too low to damage the structure.

Section II.E: G.H. Johnson, R.D. Schrimpf, K.F. Galloway, and R. Koga, "Temperature Dependence of Single-Event Burnout in N-Channel Power MOSFETs," accepted for presentation at the 1992 IEEE Nuclear and Space Radiation Effects Conference.

This paper shows that the single-event burnout susceptibility of power MOSFETs decreases with increasing temperature. This is caused by a reduction in the impact ionization rate at elevated temperature, due to increased phonon scattering.

II.B Simulating Single-Event Burnout of N-Channel Power MOSFETs

SIMULATING SINGLE-EVENT BURNOUT
OF N-CHANNEL POWER MOSFET's[†]

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ABSTRACT

Heavy ions are ubiquitous in a space environment. Single-event burnout of power MOSFET's is a sudden catastrophic failure mechanism that is initiated by the passage of a heavy ion through the device structure. The passage of the heavy ion generates a current filament that locally turns on a parasitic NPN transistor inherent to the power MOSFET. Subsequent high currents and high voltage in the device induce second breakdown of the parasitic bipolar transistor and hence meltdown of the device. This paper presents a model that can be used for simulating the burnout mechanism.

I. INTRODUCTION

The double-diffused metal oxide semiconductor (DMOS) power device is capable of conducting large currents when turned on and withstanding large voltages when turned off [1]. As system designers began using DMOS devices for space applications, heavy ion-induced single-event burnout (SEB) was identified as a catastrophic failure mechanism [2]. Following SEB, the drain and source contacts of the MOSFET are typically shorted together, and the device can no longer function as a switch. If SEB were to occur in the power supply system of a satellite or a high altitude aircraft, the results could be catastrophic.

Since heavy ions are always present in space [3], devices operating in this environment should be designed to be immune to their effects. An overview of the SEB mechanism in the DMOS device is presented in Section II of this paper. It will be shown that the SEB mechanism can be seperated into two parts: (1) the initial heavy ion-induced current filament which drives the parasitic BJT, and (2) the feedback mechanism inherent to the parasitic BJT. The heavy ion-induced current filament is discussed in Section III of this paper. The feedback mechanism determines whether the transient currents in the parasitic BJT will regeneratively increase until burnout occurs or whether the currents decrease to zero. The feedback mechanism is presented in Section IV of this paper where the operation of the parasitic BJT is discussed. The two parts of the SEB mechanism are then combined in Section V to determine the SEB threshold in terms of the linear energy transfer (LET) of the incident ion for a given device structure and operating conditions . Finally, conclusions of this work are drawn in Section VI.

II. BURNOUT MECHANISM

Before the SEB mechanism is presented, the DMOS structure will be described [1]. The cross-section of one cell in an n-channel DMOS power transistor is shown in Figure 1. This device is termed double-diffused for the manner in which it is fabricated. Both the source and the body are diffused using the gate as a mask edge. The channel length is then determined by the difference in diffusion rates of the dopants, rather than by photolithography limitations. Relatively short channel lengths, on the order of 1mm, can be obtained in this fashion. Since this is an n-channel device, a positive bias applied to the gate will invert the body region under the gate, allowing electrons to flow from the source to the drain.
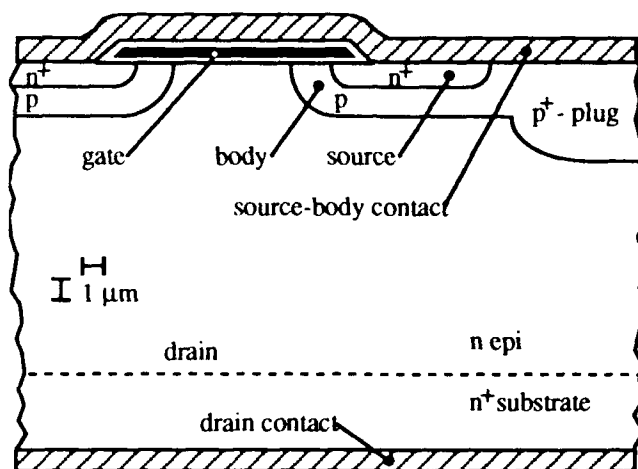

Figure 1: Cross section of a typical DMOS cell.

The most apparent difference between the DMOS device and a lateral MOSFET is that the contact to the drain is made on the bottom surface of the device, rather than on the top surface as in the lateral MOSFET. The rather thick epitaxial drain region is required to drop the large drain to source voltages that the power transistor must block while operating in the *OFF* state. When contact is made to the drain through the bottom surface metallization and the n+ substrate, the electric field lines can extend along the entire thickness of the epitaxial layer to drop the applied voltage [1].

That explains how the DMOS device can withstand high voltages, but what about the high currents? A power transistor must be able to draw large amounts of current while in the *ON* state. This is achieved by connecting thousands of the DMOS cells in parallel. This parallel combination effectively creates a very wide channel while retaining the same channel length of the individual cell, enabling a large current flow with the same applied gate to source voltage.

All real devices are not without their parasitic elements, and the DMOS structure is certainly no exception. Inherent to the DMOS structure is a parasitic npn bipolar transistor, as shown in Figure 2. The
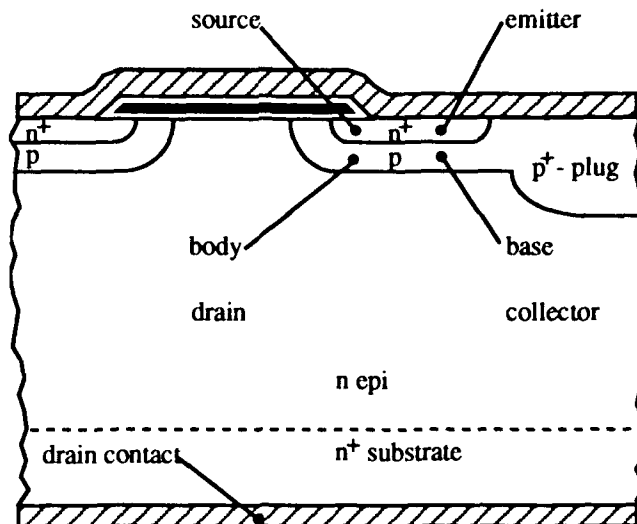
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Figure 2: Parasitic npn transistor inherent to DMOS structure.

source, body, and drain regions of the MOSFET comprise the emitter, base, and collector regions of the parasitic BJT, respectively. In normal operation of the power MOSFET, this parasitic BJT is always turned off. This is accomplished by the common source-body metallization, which shorts out the base-emitter junction of the parasitic BJT.

If lateral current flows in the body (base) below the source (emitter) region, the base-emitter junction can become forward biased and the parasitic BJT can turn on. If the parasitic BJT turns on while the power MOSFET is in the *OFF* state, the simultaneous high voltage and high current imposed on the parasitic BJT could induce second breakdown. This was the motivation for the prominent p$^+$-plug region of the DMOS structure[4]. Many power MOSFET applications require the device to switch currents through highly inductive loads. This can result in large current spikes while in the *OFF* state. These current spikes are directed through the p$^+$-plug regions and not through the parasitic BJT because of the lower impedance path. This prevents second breakdown of the parasitic BJT, and hence damage to the power MOSFET, when switching inductive loads .

Single-event burnout of the DMOS structure has been attributed to this parasitic BJT [5]. If the parasitic BJT is turned *ON* when the MOSFET is turned *OFF*, second breakdown of the BJT, and hence thermal meltdown, may occur. The mechanism leading to SEB will now be briefly discussed. Figure 3 shows the DMOS structure with a heavy ion passing through the parasitic BJT. As the heavy ion traverses the device, electron-hole pairs are generated along its track length creating an ionized plasma filament. This plasma filament supports a short-lived current sou   in which holes flow up towards ground via the lateral base region, and electrons flow down towards the collector. The short-lived current source initially drives the parasitic BJT locally turning on one cell of the DMOS structure [6].

Depending on how "hard" the BJT is initially turned *ON*, the currents within the device will either regeneratively increase until burnout occurs, or the currents will die out leaving the device unharmed.
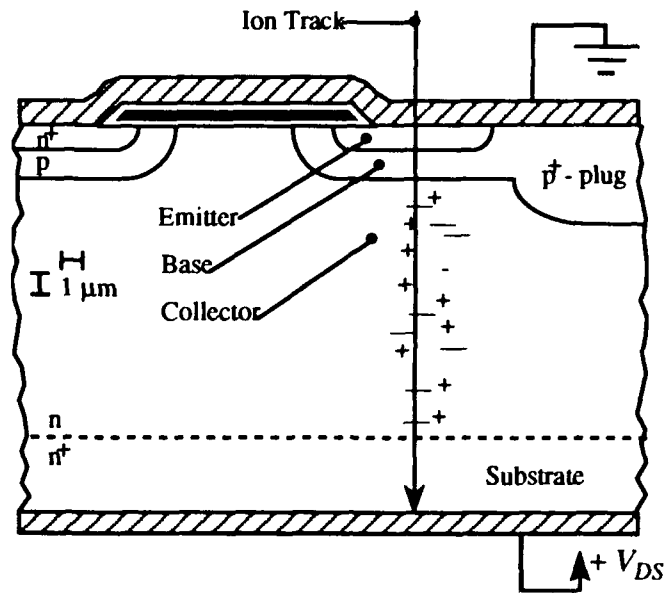
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Figure 3: DMOS structure with heavy ion track.

A feedback mechanism inherent to the vertical structure of the parasitic BJT will determine whether the currents will increase or decrease. The feedback mechanism consists of four basic components. These components in terms of the parasitic BJT are: (1) electron injection from the emitter across the active base into the collector; (2) avalanche-generated hole current returning from the collector into the base; (3) subsequent lateral hole current through the base to its contacts; and (4) the induced base-emitter voltage resulting from this lateral base current. The details of each part in the SEB mechanism will be discussed in the sections to follow.

III. HEAVY ION-INDUCED CURRENT FILAMENT

The parasitic BJT is turned on by a localized current source generated by the passage of the heavy ion. This heavy-ion-generated current filament will be referred to as the initial current source henceforth. This section will discuss the time evolution of the initial current source.

The evolution of the initial current source is governed by: (1) the kinetic energy of the incident ion and its stopping power in silicon [7]; (2) the diffusion coefficients and mobilities of carriers within the plasma filament (carriers along the ion track); and (3) the impurity profiles and operating conditions of the parasitic BJT [5]. The kinetic energy and stopping power of the incident ion determine the number of electron-hole-pairs (ehp's) generated in the silicon. The diffusion coefficients and carrier mobilities within the plasma filament determine the rate at which the ehp's generated along the ion track will diffuse radially into the silicon. The impurity profiles and operating conditions of the parasitic BJT determine the initial strength of the current source. Each of these three points will now be expanded upon.

The number of ehp's generated in a given target material due to the passage of a given heavy ion is a function of the incident ion's energy and species and of the target material. One can relate the kinetic energy of an incident ion to a quantity called its stopping power using a model developed by Ziegler [8]. The stopping power of an ion is a measure of the energy lost by the passing ion and deposited in the target material. Stopping power has units of energy per distance (i.e., MeV/µm). The energy deposited in the target material results in ehp generation. In silicon, the energy required to generate an ehp, E_p, is equal to 3.6 eV.[9] To obtain the number of ehp's per track length of the incident ion, one simply divides the stopping power, S, by 3.6 eV:

$$N_p = \frac{S}{E_p} \left[\frac{ehp}{\mu m} \right],$$ (1)

where S has the units of eV/µm. For example, the stopping power in silicon is 6.3 MeV/µm for a 150 MeV iron ion. Application of equation (1) yields ehp/µm for this incident ion.

Initially, the electron-hole pairs are generated along the ion track, creating a steep carrier gradient in the silicon. Carriers will tend to diffuse away from their initial position along the ion track due to this steep gradient. To obtain an analytically tractable model for the time evolution of the generated ehp's, the carrier plasma is approximated as a uniform line source at time t=0 that diffuses radially with a constant diffusion coefficient. This constant diffusion coefficient is approximated by [10]:

$$D \approx \frac{kT}{2q} (\mu_n + \mu_p) \approx 20 \frac{cm^2}{s}.$$ (2)

It is also assumed that the radial and axial motion of the carriers are totally decoupled and may then be treated independently. With this assumption, the time evolution of the radial profiles of the ion-generated electrons , n_p , and of the ion-generated holes, p_p, can be expressed as [11]:

$$n_p(r,t) = p_p(r,t) = \frac{N_p}{4\pi D t} exp \left[-\frac{r^2}{4Dt} \right]$$ (3)

This equation is a Gaussian function in r, with a peak concentration occurring at $r=0$. It should be noted that the peak carrier concentrations decrease with time, as one would expect. We can rearrange equation (3) to get an expression for the radius of a given concentration, N_{BC_i}, versus time:

$$r_i(N_{BC_i}, t) = \sqrt{4Dt \left[-ln \left(\frac{4\pi Dt N_{BC_i}}{N_p} \right) \right]}.$$ (4)

The terms in equation (4) are identical to those in equation (3) with the exception that N_{BC_i} has
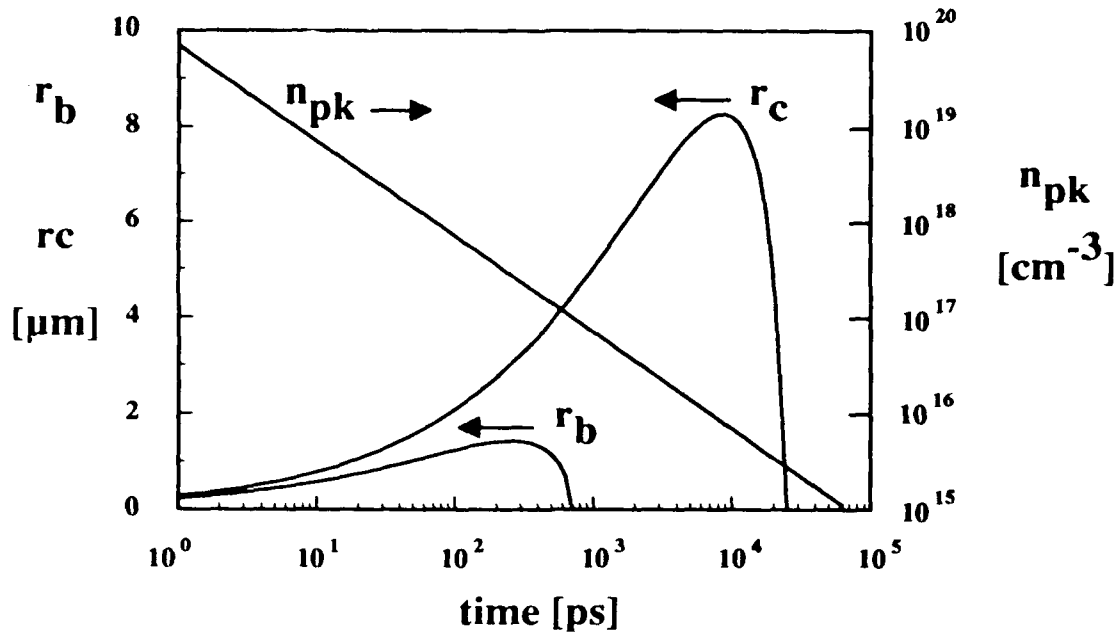
Figure 4: Radii of core regions corresponding to and and peak carrier concentration of the plasma filament resulting from a 150MeV Fe ion.

replaced n_p or p_p. In Figure 4, equation (4) is plotted for the two radii, r_b and r_c, versus time for the two concentrations $N_{BCb} = 10^{17} \text{cm}^{-3}$ and $N_{BCc} = 10^{15} \text{cm}^{-3}$. These concentrations correspond to base and collector doping densities in a typical parasitic BJT. Equation (3), for the case of $r=0$, is also plotted in Figure 4. As shown in Figure 4, both radii grow to a maximum and then decay to zero, while the peak concentration decays to N_{BC_i} when the corresponding radius shrinks to zero. The importance of these properties of various radii will become apparent when carrier densities that are able to turn on the parasitic BJT are discussed.

Several other interesting and important relationships can be developed using equations (3) and (4). One relationship that will be useful in determining the current within a core region of radius r_i is the total number of carriers contained within that core per unit core length. The core length is in the same direction as the ion track. Integration of equation (3) from 0 to r_i yields:

$$N(r_i) = N_p \left[1 - exp \left(\frac{r_i^2}{4Dt} \right) \right] = N_p - 4\pi Dt N_{BC_i}. \tag{5}$$

Another interesting relationship that gives the time at which a particular radius, r_i, vanishes can be found by setting equation (2.4) to zero and solving for t. The result is:

$$T_i = \frac{N_p}{4\pi D \, N_{BC_i}}. \tag{6}$$

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Equations (3) - (6) describe aspects of the time evolution of the heavy-ion-generated electron-hole-pairs. One more issue must be resolved before an expression for the current within the plasma filament can be written. With typical power MOSFET drain-to-source voltage ratings of 50 V to 500 V, and typical distances between drain and source contacts in the tens of microns range, the electric fields throughout much of the collector depletion region will be above the saturation field, E_{sat}[5]. In silicon, $E_{sat} = 100\,kV/cm$ [12]. This causes the holes and electrons to drift at saturation velocity, which is taken to be $v_{sat} \approx 10^7 cm/s$ for both electrons and holes.[12] Thus, the current within a core region defined by r_i is simply the product of the saturation velocity and the total charge per unit length. This current is given by:

$$I_i = q\,v_{sat}N(r_i). \tag{7}$$

Equation (7) gives the total current within a core region defined by r_i, which corresponds to a particular carrier concentration level. In light of equations (3) - (7), the instantaneous current density within a core region is constantly changing. Somewhere between the uniform line source created by the heavy ion strike and the totally diffused plasma filament lies this initial source that acts to turn on the parasitic BJT. The parasitic BJT has a finite turn on time, τ_{on}. The value of the initial current source at time, τ_{on}, will be used as the current that drives the parasitic BJT. The resulting current that drives the parasitic BJT is expressed as:

$$I_{on} = q\,v_{sat}N(r_c,\,\tau_{on}). \tag{8}$$

IV. PARASITIC BJT OPERATION

This section will address the operation of the parasitic BJT following an ion strike. First, the feedback mechanism that governs whether the currents within the parasitic BJT will regeneratively increase or die out to zero will be discussed. In the development of the feedback mechanism, it will become apparent that an expression for avalanche-generated hole current in the base-collector space charge region (SCR) the parasitic BJT is necessary. This relationship will be described in this section. Finally, the turn-on time of the parasitic BJT will be discussed.

IVA. FEEDBACK MECHANISM

Depending on how hard the parasitic BJT is initially turned on, currents within the device will either: (1) regeneratively increase until the simultaneous high current and high voltage in the device trigger second breakdown and consequently thermal meltdown; or (2) the currents will die out to zero leaving the device unharmed. A feedback mechanism inherent to the device structure dictates whether
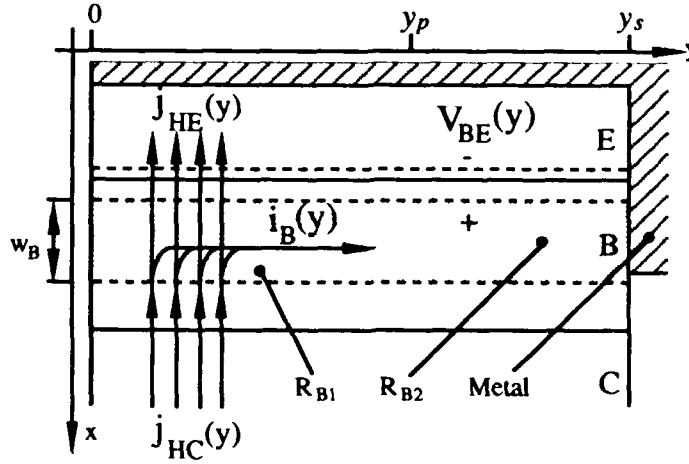
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Figure 5: Feedback model of parasitic bipolar junction transistor.

the currents will regeneratively increase or decrease.

The feedback mechanism relates: (1) electron injection from the emitter across the active base into the collector; (2) avalanche-generated hole current returning from the collector into the base; (3) subsequent lateral hole current through the base to its contacts; and (4) the induced base-emitter voltage resulting from this lateral base current [14]. The equations governing the feedback mechanism will now be discussed.

The coordinate system for this discussion is shown in Figure 5. The origin is defined at the point of the ion strike. The regions labelled E, B, and C are the emitter, base, and collector of the parasitic BJT. The region R_{B2} in the base is the p$^+$ plug region, and the region R_{B1} is the p body region. The length of the source region in the y direction is defined as y_s, and the p-body p$^+$ plug interface is defined as y_p. The extent that the p$^+$ plug extends under the n$^+$ source region, y_e, is difined as the difference between y_s and y_p.

Now, assuming a potential, $V_{BE}(y)$, exists that is large enough to locally turn on the parasitic BJT, the electron current density injected by the emitter, $j_{EC}(y)$, can be expressed to first order by [15]:

$$j_{EC}(y) = \frac{q\,D_n\,n_i^2}{N_{AB}\,w_B}\exp\left[\frac{V_{BE}(y)}{kT/q}\right], \tag{9}$$

where $q, D_n, n_i, N_{AB}, w_B, k$, and T correspond to the electronic charge, electron diffusivity, intrinsic doping density, doping density in the base region, active base width , Boltzman constant, and absolute temperature, respectively. Note that this current density is not shown in Figure 5 to avoid confusion.

Since the base-collector junction has a large reverse bias applied across it, the electric field will be large throughout much of the collector region. Therefore, for each electron injected across the base into the collector, there will be avalanche-generated holes returning to the base region. The avalanche-

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generated hole current density, $j_{HC}(y)$, is given by [14]:

$$j_{HC}(y) = M \, q \, v_{sat} \left\{ \frac{D_n \, n_i^2}{v_{sat} N_{AB} \, w_B} \exp\left[\frac{V_{BE}(y)}{kT/q}\right]\right\}, \qquad (10)$$

where v_{sat} is the saturation velocity for electrons. The multiplication factor, M, in equation (10) is defined as the ratio of the hole density to the electron density at the base side of the base-collector space charge region (SCR). M is a function of the electric field, ionization rate, and the injected electron density, and is obtained numerically [14]. The multiplation factor, M, will be discussed later in this section. The term within the curly brackets in equation (10) is the electron density at the base edge of the base-collector SCR, including the Kirk effect [16].

Due to the forward bias, $V_{BE}(y)$, there also exists a back-injected hole current density, $j_{HE}(y)$. This current density is expressed to first order by [15]:

$$j_{HE}(y) = \frac{q \, D_n \, n_i^2}{N_{DE} L_p} \exp\left[\frac{V_{BE}(y)}{kT/q}\right], \qquad (11)$$

where D_p, N_{DE}, and L_p correspond to the diffusivity of holes, the doping density in the emitter, and the diffusion length of holes, respectively.

There is one remaining current in the feedback mechanism to be described. This is the incremental hole current density which flows laterally through the neutral base region to the ground contact and develops the Ohmic drop necessary to keep the base-emitter junction forward biased. The value of this incremental current density, $j_{HB}(y)$, at any point y is simply the difference between the avalanche-generated hole current density and the back-injected hole current density, which is:

$$j_{HB}(y) = j_{HC}(y) - j_{HE}(y). \qquad (12)$$

A second order differential equation can be formulated that relates the Ohmic drop to the current density in the neutral base region [14]. First, the incremental lateral base current is just the local incremental base current density:

$$\frac{d \, i_B(y)}{d \, y} = j_{HB}(y). \qquad (13)$$

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Second, the incremental voltage drop is given by:

$$\frac{d\,V_{BE}(y)}{d\,y} = -R_B(y)\,i_B(y).$$

(14)

Equations (13) and (14) can be combined to give:

$$\frac{d^2\,V_{BE}(y)}{d\,y^2} = -R_B(y)\,j_{HB}(y).$$

(15)

Equations (10) - (12) and (15) can be solved to obtain a critical condition necessary to initiate burnout [14]. This calculation will be illustrated for a specific device structure. Note that this calculation will involve numerically obtained values of the avalanche multiplication factor, M.

The critical condition will now be calculated for a typical DMOS structure. The following parameters are used in the calculations: source doping density = 2×10^{20} cm^{-3}, p- body doping density = 2×10^{16} cm^{-3}, p$^+$ plug doping density = 2×10^{18} cm^{-3}, drain doping density = 1.1×10^{15} cm^{-3}, source diffusion depth = 1 μm, p- body diffusion depth = 2 μm, p$^+$ plug diffusion depth = 4 μm, and epitaxial layer thickness = 22 μm. The average doping densities needed in this abrupt junction calculation were obtained from Gaussian-type doping profiles.

The solution to equations (10)-(12) and (15) is shown in Figures 6-8. The collector bias for this case is 250V. Shown in Figure 6 is the incremental hole current density profile in the base region. The base current per gate width is shown in Figure 7, and the base-emitter voltage is shown in Figure 8. These
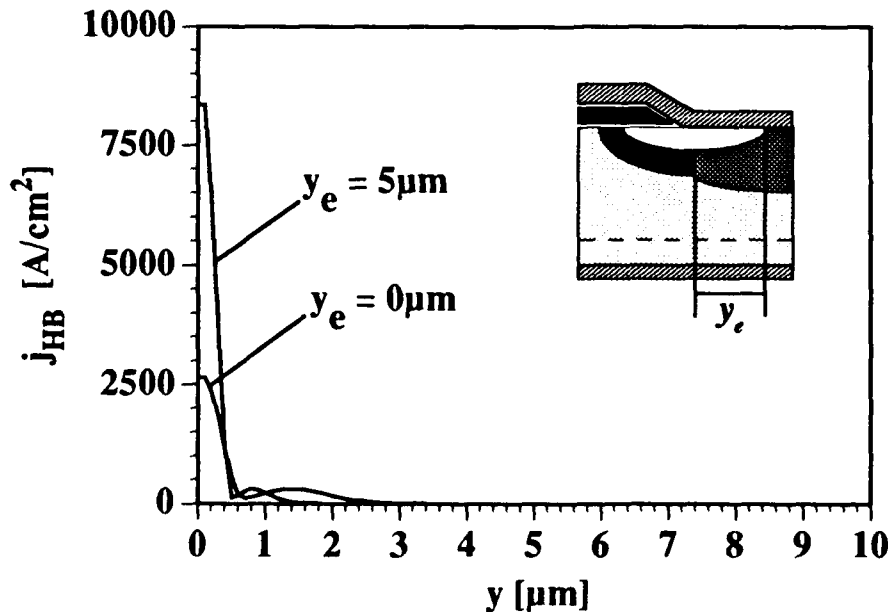

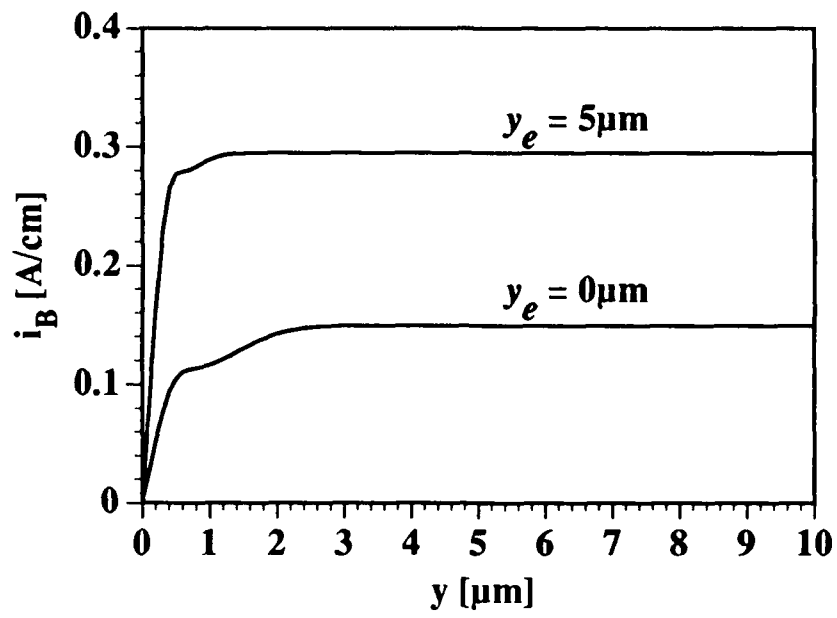Figure 6: Critical incremental base current density for burnout.

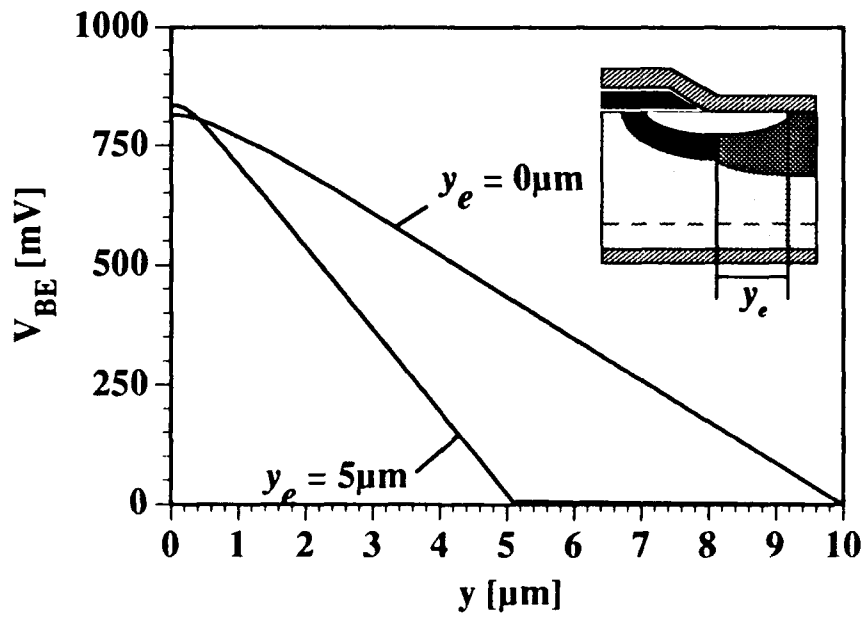Figure 7: Critical base current density for burnout.

Figure 8: Critical base-emitter voltage for burnout.

curves represent the critical condition for burnout because any heavy-ion generated perturbation in the system larger than that given in Figures 6-8 will result in regeneratively increasing currents within the device and thus burnout occurs [14]. If the heavy-ion generated perturbation is less than that given in Figures 6-8, the currents will decay to zero; and burnout does not occur.

IVB. AVALANCHE-GENERATED HOLES

This section of the paper will discuss the avalanche multiplation factor, M, which appears in the equations governing the feedback mechanism. As mentioned previously, M is a function of the electric field, impact ionization rate, and electron density within the base-collector SCR. The complete details of this calculation appears in [14]. Only the major points will be described here. The one dimensional Poisson equation will be solved across the base collector depletion region taking into account the space charge associated with the mobile carriers.

When the space charge of the mobile carriers is considered, the electric field across the base collector space charge region will be somewhat altered, depending on the density of mobile charge
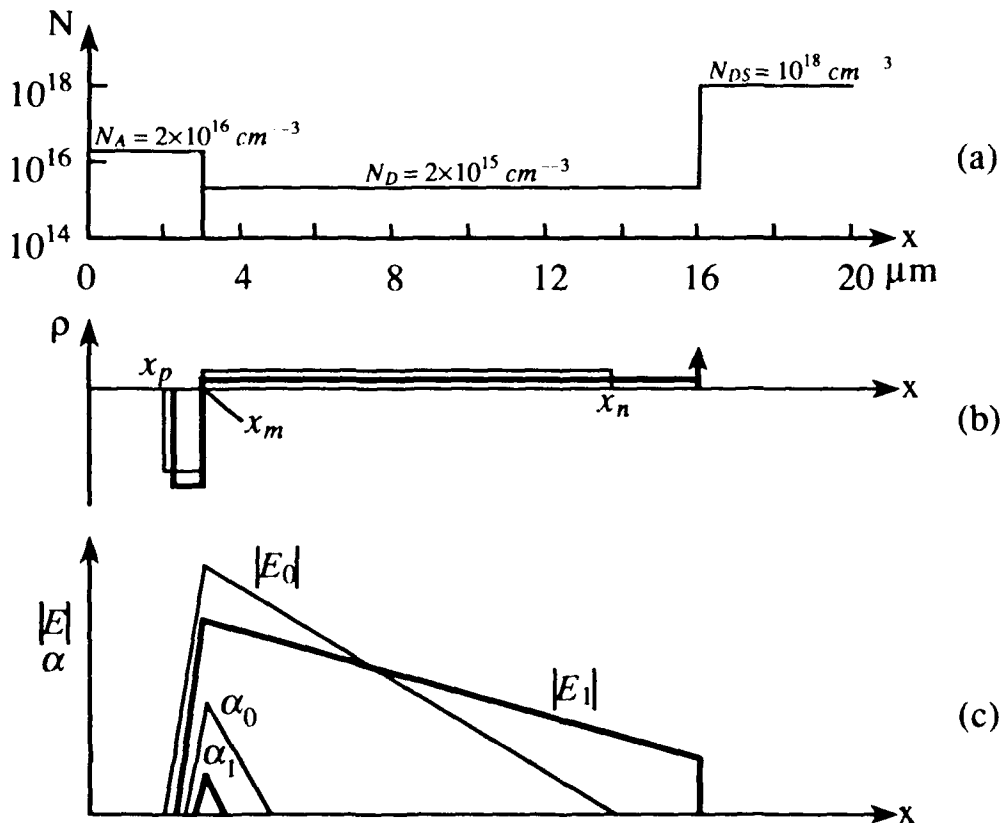
Figure 9: (a) Approximated pnn+ impurity profile. (b) Charge density in space charge region for zero and non-zero currents. (c) Electric field and ionization rate in space charge region for zero and non-zero currents.

compared to the density of background impurity charge. A qualitative illustration of how the electric field is changed is shown in Figure 9 [14]. An idealized impurity profile through the base, collector, and substrate of the parasitic BJT in a typical power MOSFET is shown in Figure 9a. The two cases of zero and non-zero current are depicted in Figures 9b and 9c. The light lines correspond to the zero current case, and the heavy lines correspond to the non zero current case. The electric field and ionization rate plots are further labelled with the subscripts 0 and 1 to distinguish between zero and non-zero currents respectively. The total charge density for the non-zero current case, shown in Figure 9b, has changed to reflect the electrons in transit across the junction. The total charge density to the left of the metallurgical junction , x_m, is more negative (the electrons add to the total charge), and the total charge density to the right of the metallurgical junction is less positive than for the zero current case (the electrons subtract from the total charge).

The change in the total charge density is also reflected in the electric field distribution, shown in Figure 9c. Since the total charge density is more negative to the left of x_m for non-zero current, the electric field in this region will have a steeper slope than for the zero current case. This effectively lowers the peak electric field at x_m and moves x_p to the right. Similarly, since the total charge density is less positive to the right of x_m for non-zero current, the electric field in this region will have less of a gradient than for the zero current case. Since the reverse bias for each case is the same, the area under each electric field plot must be equal. This equal area constraint and the lower slope to the right of x_m, push the right edge of the electric field, x_n, deeper into the collector region. In the example shown in Figure 9c, x_n, has reached the epi-substrate boundary at which point the electric field can penetrate no further. The electric field will assume a non-zero value at the epi-substrate boundary to satisfy the equal area constraint imposed by the Poisson equation. Therefore, two important phenomena occur in the reverse biased base collector junction when non-zero current flows: (1) the peak electric field at the metallurgical junction decreases, and (2) the electric field assumes a non-zero value at the epi-substrate interface. These two consequences significantly affect the avalanche multiplication, as will be shown later.

The impact ionization rate, α, throughout the depletion region for zero and non-zero current is also shown in Figure9c. The functional dependence of α is exponentially related to the local electric field. This is why the value of α decreases significantly when the peak electric field drops with increasing current. We would expect the avalanche multiplication rate to significantly decrease with increasing current as well. The functional relationships between carrier densities, electric field, ionization rate, applied voltage, and the physical geometry of the parasitic BJT must be simultaneously solved to more precisely determine the avalanche multiplication rate.

Recall that the desired result is the hole concentration at x_p, $p(x_p)$, as a function of electron concentration at x_p, $n(x_p)$, or:
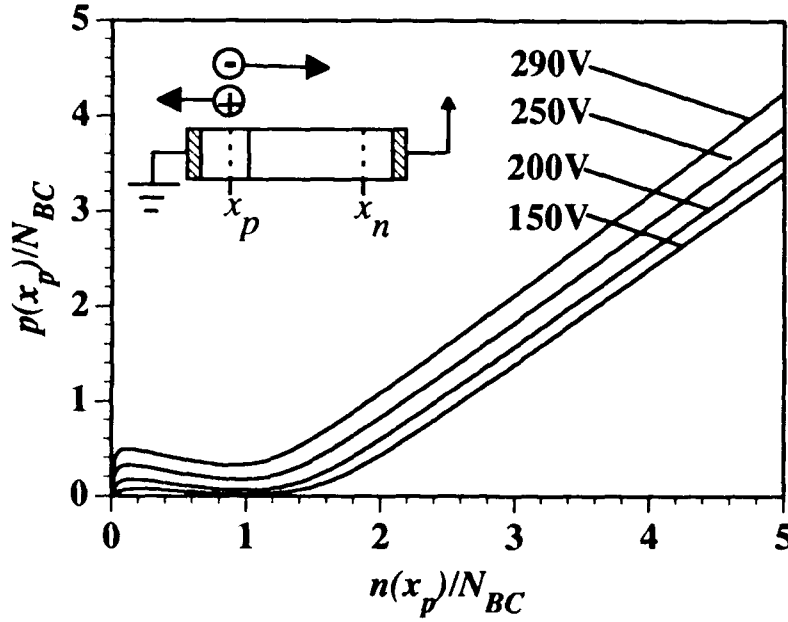
$$M = \frac{p(x_p)}{n(x_p)}. \tag{16}$$

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Figure 10: Avalanche curves: normalized hole concentration at xp vs. normalized electron concentration at xp, for different values of VDS.

There are six arrays of typically 300 points used in the calculation. These arrays are: (1) space charge, $\rho(x)$; (2) electric field, $E(x)$; (3) potential, $V(x)$; (4) ionization rate, $\alpha(x)$; (5) electron concentration, $n(x)$; and (6) hole concentration, $p(x)$. Given the impurity profile, the applied drain to source voltage, V_{DS}, and the electron concentration at x_p, the profiles of $\rho(x)$, $E(x)$, $V(x)$, $n(x)$, $p(x)$, and $\alpha(x)$ are calculated for self-consistency [14].

The equations, sample calculations of electric field, ionization rate, potential, carrier densities, and other details of this calculation appear in [14]. The end result is plotted in Figure 10. There are three distinct regions present in each avalanche curve shown in Figure 10. The first region is the distinct hump appearing for values of $n(x_p)/N_D < 1$. This corresponds to an initial decrease in the avalanching rate with increasing current. The second region is the valley region or local minimum appearing for values of $n(x_p)/N_D \approx 1$. This corresponds to a near zero avalanching rate at a current level where the electron density and collector doping density are comparable. The third region of the avalanche curve appears for values of $n(x_p)/N_D > 1$, where the hole concentration increases at approximately the same rate as the electron concentration.

In terms of the feedback mechanism for SEB, the appropriate value for M can be obtained from a curve similar to Figure 10. Note that it is necessary to calculate a separate avalanche curve for each device structure and each applied drain-source bias when solving the equations governing the feedback mechanism.

IVC. TURN-ON TIME OF PARASITIC BJT

The turn on time, τ_{on}, of the parasitic BJT can be approximated by the sum of the emitter capacitance charge-up time τ_E, the base transit time τ_B, and the collector transit time τ_C[5]:

$$\tau_{on} = \tau_E + \tau_B + \tau_C,$$ (17)

$$\tau_E = r_E \, C_{TE} = \frac{V_T}{j_{EC}} \sqrt{\frac{q \varepsilon N_{AB}}{V_{BI}}},$$ (18)

$$\tau_B = \frac{w_B^2}{2 \, D_n},$$ (19)

and

$$\tau_C = \frac{w}{v_{sat}},$$ (20)

where V_{b_i} is the built-in potential of the emitter junction, w_B is the active base width, and w is the thickness of the epitaxial layer under the base region. The estimated turn-on time for the structure used in calculating the critical condition is: $\tau_{on} = 1ps + 82ps + 200ps = 283ps$.

V. CALCULATED BURNOUT THRESHOLDS

Now that each part of the model has been developed, the burnout threshold for a particular device may be calculated. The burnout threshold will be defined in terms of the linear energy transfer (LET) of the incident ion. The LET is simply the stopping power divided by the volume mass density of the target material (i.e. silicon in this case). The LET will be expressed in units of MeV-cm²/mg for these calculations.

It is necessary to compare the magnitude of the current in the plasma filament at time ton with the critical condition for burnout given by the feedback mechanism. Given the V_{BE} profile in Figure 8, one can readily calculate the corresponding electron current density in the collector, j_{EC}. This is shown in Figure 11. To find the electron current in the collector given by the feedback mechanism, the current density shown in Figure 11 must be integrated over one cell in the DMOS structure. A top view of the DMOS structure is shown in Figure 12 for a square cell geometry. An actual DMOS device may incorporate a different cell geometry (i.e. hexagonal), but a square geometry is sufficient for this discussion.
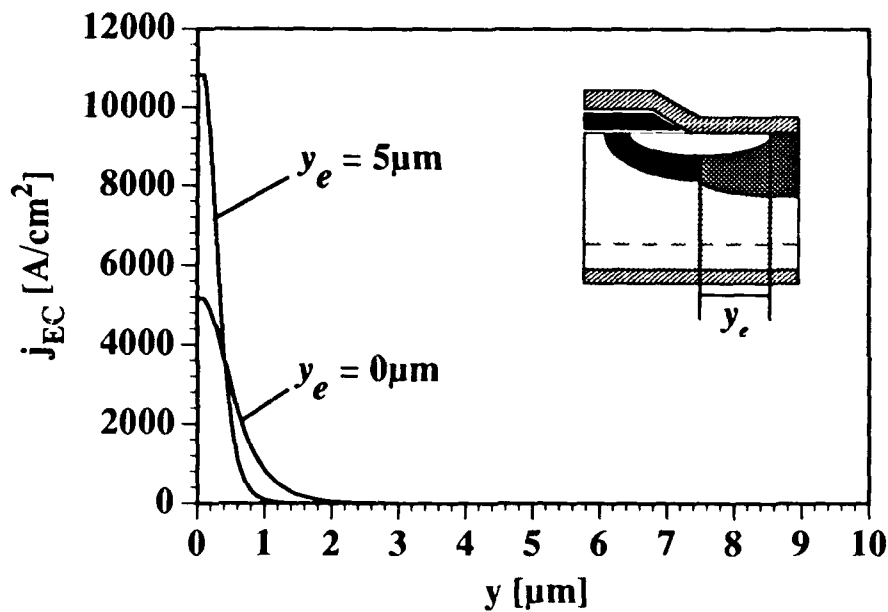
Figure 11: Critical collector current density for burnout.
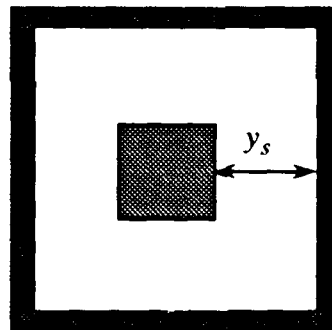
Figure 12: Top view of a DMOS cell with metallization and gate regions omitted.

The integration of the electron current density in the collector over the DMOS cell is approximated in the following manner. First, the current density is numerically integrated in the y direction of Figure 11. This result is then multiplied by the perimeter of the of the n^+ source region shown in Figure 12. This perimeter will equal 120µm in the following calculations. The current that is calculated in this

fasion is defined as the critical current for burnout. In other words, if the ion strike results in a current greater than the critical current, then the transient currents within the parasitic BJT will regeneratively increase until second breakdown sets in. If the ion strike results in an initial current less than the critical current, then the transient currents within the parasitic BJT will die out to zero.

The following algorithm is used to calculate the LET burnout threshold for a given DMOS structure: (1) Given the structural parameters and drain-source voltage, the critical condition is calculated as in Section VA; (2) Given the critical condition, the critical electron current density in the collector is calculated; (3) Given the critical collector current density, the critical current is calculated as described above; and (4) Equation (8) at time ton is used to calculate the LET necessary to initiate the critical current. A non-ideal scaling factor, γ, can be introduced at this point. This factor may be used to scale part (4) in the above algorithm when comparing to part (3). In this fasion, the model can be fitted to measured data. The device structure that will be used in the following calcualtion is that used for finding the critical condition in Section VA, with one exception. The lateral extent of the p^+ plug, y_e, where

$$y_e = y_s - y_p, \tag{21}$$

(i.e. the length that it extends under the n^+ source as shown in Figure 5) will be varied. For example $y_e=0$ μm means that the p^+ plug does not extend under the source region and $y_e=5\mu$m means that the p^+ plug extends 5 μm under the source region.

The LET burnout threshold is calculated as a function of y_e and V_{DS} using the algorithm above with $\gamma=0.2$. The results of this calculation are shown in Figure 13, where y_e is varied from 0μm to 8μm and V_{DS} is varied from 150V to 290V.

VI. DISCUSSIONS AND CONCLUSIONS

The information contained in Figure 13 can be helpful in designing a DMOS device to be more resistant to SEB. The LET burnout threshold for a given device structure increases with increasing ye for a fixed drain-source bias. As one increases the extent that the p^+ plug extends under the source (emitter), i.e. increases y_e, the total resistance seen in the base region of the parasitic BJT decreases. When incorporated into the feedback mechanism, this necessitates higher current densities in the base region for the critical solution. (i.e. the lower resistance requires a higher current to drop a comparable voltage) This suggests that the p^+ plug should extend as far as possible below the source region to prevent burnout. The p^+ plug can not extend so far as to influence the threshold voltage of the MOSFET, however. Figure 16 also indicates that the LET burnout threshold decreases with increasing drain-source bias for a given device structure with y_e held constant. This is due to the higher electric fields associated with the increased drain-source bias. Higher electric fields increase the impact ionization rate and hence the avalanche-generated hole current that flows to the base region from the collector region of the parasitic
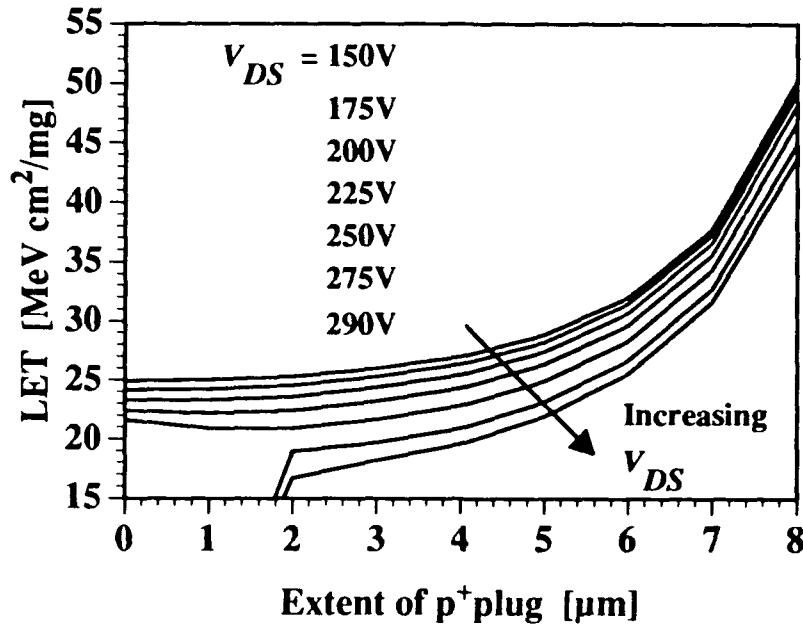
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Figure 13: LET burnout threshold as a function of y_e and V_{DS}.

BJT. (i.e. more current is generated within the device for the same base-emitter bias) Therefore, when included in the feedback mechanism, the current required to initiate burnout decreases with increasing drain-source bias. Note that the drain-source bias dependence on the LET burnout threshold is less than the parasitic base resistance dependence.

In summary, a method for simulating single-event burnout of n-channel power MOSFETs has been described. The model was divided into two parts: (1) the heavy ion-generated current source; and (2) the feedback mechanism inherent to the parasitic bipolar transistor. It was shown that the feedback mechanism, which related transient currents and voltages in the parasitic BJT, could be solved for a critical solution for burnout. If the currents given by the critical solution are exceeded by the heavy ion-generated current source at the turn on time of the parasitic BJT, then currents would regeneratively increase. The simultaneous increasing high currents and voltages trigger second breakdown of the bipolar and finally meltdown of the DMOS structure. If the initial current source does not exceed the currents given by the critical solution, then the transient currents in the parasitic BJT will die out to zero. Finally, the simulation results indicate that the LET burnout threshold increases when the p+ plug is expanded farther under the source region, and that the LET burnout threshold decreases with increasing drain-source bias.

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II.C Analytical Model for Single-Event Burnout of Power MOSFETs

ANALYTICAL MODEL FOR SINGLE EVENT BURNOUT OF POWER MOSFETS *

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Abstract

The processes causing single event burnout in power MOS-FETs are modeled analytically, describing the evolution of the plasma-filament from an ion traversing the structure and the processes constituting the triggering mechanism of second breakdown. Analytically tractable models are achieved by employing simplifying approximations in common use in established semiconductor device theory, and by using initial conditions and parameters typical for simulations of single event upset phenomena. Comparative simplicity and tractability is favored over accuracy to gain lucid relationships between pertinent parameters, which can guide device design and optimization, aid the interpretation of results from simulation and experiment, and help in the development of simulation software.

1. Introduction

This paper reports on an analytical study of the mechanisms leading to single event burnout in power MOSFETs. The processes are described in terms of the characteristics of the traversing particle — mass, kinetic energy and stopping power — and of the physical and operating parameters of the transistor — impurity profiles, horizontal dimensions and drain-to-source voltage. A collection of analytically tractable models for individual mechanisms at work is achieved by making the same simplifying assumptions that underlie the analytical transistor models in common use, and by using initial conditions and parameters typical for simulations of single event upset phenomena.

In deriving analytical models, one is faced with choices between accurate, but complex representations, and simpler and more easily tractable but less accurate descriptions. In this first order analysis, relative simplicity and tractability is favored in order to enhance insight. The models are applied to a particular transistor structure and to two ion tracks of vastly different carrier concentrations in order to obtain an idea of the magnitudes of the parameters involved. The numerical results are typically given to two significant digits to maintain internal accuracy in the models, with no intention to suggest that the models describe reality that closely. The main objective of this study is to establish sensitivities of the single event upset mechanisms to individual transistor parameters.

The analysis is limited to vertical ion tracks through the power MOSFET structure depicted in Fig. 1. At least two mechanisms can lead to burnout.

(1) An ion that traverses the transistor through the gate, but avoiding the p-regions generates a plasma-filament through the n-epi region of the collector. This filament locally shorts the potential drop across the drain depletion region and applies the drain potential directly to the gate oxide. If the potential difference between drain and gate is large enough to break down the gate oxide, sufficient power can be delivered to the breakdown region to thermally destroy the gate. (This mechanism is not investigated further in this paper.)

(2) An ion that traverses the transistor structure through the source turns on the parasitic npn-transistor below the source
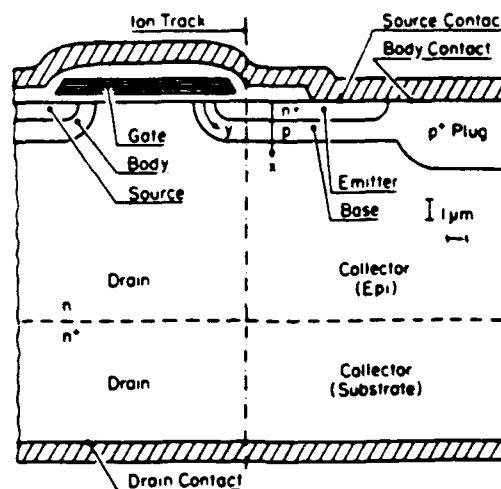
Figure 1: Power MOSFET structure.

region. When this occurs while the MOSFET is operated with a drain voltage that exceeds BVCER of that transistor region, a condition called second breakdown can occur. BVCER is the collector-emitter breakdown voltage of a bipolar transistor, the base of which is connected to the emitter through a moderate conductance. Depending on the value of this conductance, BVCER varies between BVCBO and BVCEO.

The second breakdown condition is well-known from early power MOSFET designs. In these transistors, it is induced, for example, when a drain voltage transient leads to avalanching on the drain side of the channel of the MOSFET proper [1,2]. The resulting hole current flows primarily through the thin p-layer to the p-contact. When this current develops a sufficient voltage drop to locally turn on the emitter diode of the npn-structure near the FET channel, the resulting collector current causes more avalanching in the collector depletion region. This regeneratively increases the hole current into the p-layer, the voltage drop across this layer, and the collector current. The current increases until the drain voltage is forced down to BVCER. The resulting excessive local power dissipation leads to destruction of the device. BVCEO typically falls between 20 and 50% of BVCBO.

The introduction of a p^+-plug below the p-contact to reduce the thickness of the n-epi region, as shown in Fig. 1, alleviates this problem at least for normal operation. The region below the plug now starts avalanching first and clamps the drain voltage to values that cause no avalanching in the channel region. The avalanche current flows vertically through the plug directly to the source contact. The potential along the p-region is not raised, and the parasitic npn transistor is nowhere turned on [3]. However, the vulnerability to single event burnout, while perhaps reduced, is basically not eliminated by the p^+-plug because it only masks the intrinsic instability of the structure. An ion track through or near the channel region can deposit ample carriers to trigger the second breakdown mechanism [4].

In Section 2, pertinent relationships between physical and electrical parameters of the parasitic npn structure are derived
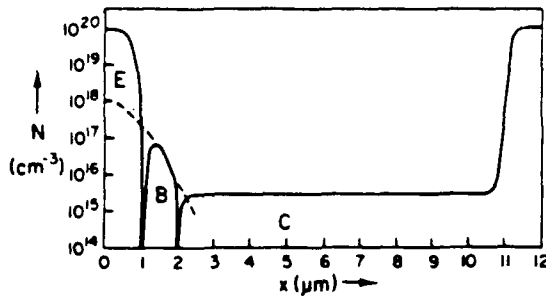
Figure 2: Impurity profile of n^+pnn^+ transistor structure.

and discussed. The structure is found to operate deeply in avalanche mode. which motivates the determination of the critical point for onset of second breakdown in Section 3. The evolution of the plasma-filament and the currents through it are analyzed in Sections 4 and 5. Section 6 is devoted to studying the operating conditions of the npn-structure in and near the plasma-filament, and to demonstrating the presence of the second breakdown mechanism. Section 7 concludes the paper with a discussion of results and conclusions.

2. Physics of the MOSFET and Parasitic NPN Structures

To focus on the problem, consider the transistor structure of Fig. 1, with the impurity profile of Fig. 2, operated with $V_D = 100V$. Elementary step-junction theory gives the drain depletion width as

$$w = [2\epsilon(N_a + N_d)V_D/(qN_aN_d)]^{1/2}, \qquad (1)$$

and, for $N_d = 3 \times 10^{15} cm^{-3}$ and an average N_a of $5 \times 10^{16} cm^{-3}$, yields $w = 6.8\mu m$. The depletion region extends by only about $0.4\mu m$ into the p-side. Hence, the approximation of the Gaussian profile by an average constant concentration causes little error in the depletion layer width and in the maximum electric field. In the step junction approximation, the electric field is zero at the edges of the depletion region and rises linearly to

$$E_{max} = 2V_D/w = \{2qN_aN_dV_D/[\epsilon(N_a + N_d)]\}^{1/2}, \qquad (2)$$

which occurs at the metallurgical junction and equals $300kV/cm$ in this example.

The high electric fields lead to pair generation by impact ionization when carriers traverse the depletion region. The number of electron-hole-pairs (ehp) generated per unit path length of a primary electron is defined as the ionization rate α. It is given, e.g.. by Sze [5] and can be approximated for electrons by

$$\alpha = A \exp{-(E_0/E)}, \qquad (3)$$

with $A = 89\mu m^{-1}$ and $E_0 = 1.2MV/cm$. The respective parameter values for holes are $260\mu m^{-1}$ and $2.0MV/cm$. which makes the ionization rates for holes much lower. Only carriers that move with saturation velocity cause noticeable pair generation.

For later developments the ehp generation profiles for two limiting electric field configurations are of interest: (1) a constant electric field across the n-epi region of the collector, w_n, and (2) the triangular field distribution of the depleted region as given by Eqns. 1 and 2. As explained in Section 5. the high carrier densities in the core of the plasma-filament lead to a constant electric field

$$E_r = V_D/w_n \qquad (4)$$

In this example. $w_n = 9\mu m$. and E_r amounts to $110kV/cm$.

Now. consider a steady flux of electrons traversing the depletion region in the x-direction. If the electron concentration at x is $n(x)$, then avalanching in the field $E(x)$ raises the concentration at $x + dx$ to $n(x + dx) = n(x)[1 + \alpha(x)dx]$, and it satisfies the differential equation

$$dn/dx = \alpha(x)n(x). \qquad (5$$

Its integration, using the field E_p leads to

$$n(x)/n(0) = \exp(\alpha x) = \exp[A \exp(-E_0/E_p)x], \qquad (6$$

and yields $n(w_n)/n(0) = 1.015$.

Integration of Eqn. 5 for the triangular field in the depletion region between x_p and $x_n > x_p$ still leads to an analytical electron concentration profile. although in terms of the exponential integral E_1. The electron profile is described by

$$n(x)/n(x_p) = \exp\{A(x_j - x_p)[(\exp -\eta) - \eta E_1(\eta)]\};$$
$$x_p < x < x_j, \qquad (7a$$

$$n(x)/n(x_p) = M_n/\exp\{A(x_n - x)[(\exp -\varsigma) - \varsigma E_1(\varsigma)]\};$$
$$x_j < x < x_n, \qquad (7b$$

$$M_n = \exp\{A(x_n - x_p)[(\exp -\eta_0) - \eta_0 E_1(\eta_0)]\}, \qquad (7c$$

with avalanche multiplication factor M_n. $\eta_0 = (E_0/E_{max})$ $\eta = \eta_0[(x_j - x_p)/(x - x_p)]$ and $\varsigma = \eta_0(x_n - x_j)/(x_n - x)$. The function (7) is plotted in Fig. 3a. For $V_D = 100V$, more than 6 electrons arrive at x_n for each primary electron entering the depletion region at x_p. Fig. 3a also shows the hole profile, which is described by

(a)
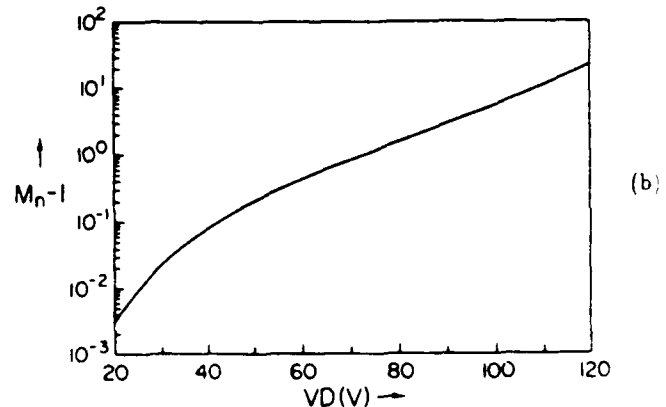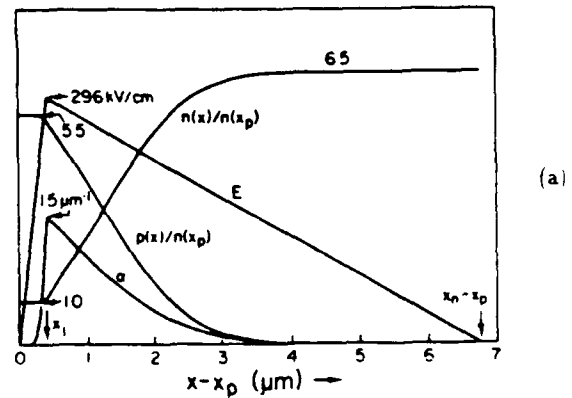

(b)

Figure 3: (a) Electric field E, ionization rate α, and electron and hole multiplication factors $n(x)/n(x_p)$ and $p(x)/n(x_p)$ in the collector depletion region. (b) Avalanche multiplication factor M_n versus collector voltage.

$$p(x) \; n(x_p) = n(x_n) \; n(x) \; n(x_f).\qquad(8)$$

For each primary electron, more than 5 holes return to the p-layer. The quantity $M_n - 1$ is plotted versus V_D in Fig. 3b. For an analogous p-channel structure only 0.3 electrons would return to the base for each primary hole, and p-channel transistors are correspondingly less prone to second breakdown and burnout, as is well established by experiments.

For the regenerative turn-on mechanism of second breakdown, the electron concentration caused by the collector current, the current gain, and the turn-on time of the parasitic npn-structure are important.

The relationships between the base-emitter voltage V_{BE}, the excess electron concentration n_{pe} at the base edge, the electron concentration n_{jc} injected into the collector depletion region, and the current density j are

$$n_{pe} = (n_i^2 / N_a)\exp(V_{BE}/V_T),\qquad(9)$$

$$j = qD_n n_{pe} / w_B = qD_n n_i^2 / (N_a w_B) \exp(V_{BE}/V_T),\qquad(10)$$

$$n_{jc} = j / (qv_{sat}) = D_n n_i^2 / (N_a w_B v_{sat}) \exp(V_{BE}/V_T),\qquad(11)$$

where $V_T = kT/q$ and D_n is the electron diffusion coefficient in the base. For example, a V_{BE} of 0.73V results in $n_{pe} = 7 \cdot 10^{15} cm^{-3}$, $j = 400 A/cm^2$ and $n_{jc} = 3 \cdot 10^{14} cm^{-3}$; the latter being an order of magnitude below N_d.

The current gain is the product of the avalanche multiplication factor M_n, the base transport factor α_T and the emitter efficiency γ, given to first order by [6]

$$\alpha = M_n \alpha_T \gamma = M_n [1 - \frac{1}{2}(w_B/L_n)^2][1 - N_a w_B / (N_{dE} L_n)].\qquad(12)$$

With the extremes of M_n given by unity and Eqn. 7c, a neutral base width $w_B = 0.5\mu m$, a donor concentration in the emitter $N_{dE} = 1 \cdot 10^x cm^{-3}$ and a low estimate of the electron diffusion length in the base of $L_n \sim 10\mu m$, one obtains $\alpha_T = 0.995$ and $\gamma = 0.9999$, and α ranges from 0.995 to 6.5. Operation is intrinsically stable only when $\alpha < 1$, which limits M_n to 1.005. Clearly, the parasitic npn-structure operates deep in the avalanche region, and the only factor preventing it from immediate avalanche breakdown is the impedance of the base layer, which shunts the excess hole current from the base to ground (one hopes). This is discussed in more detail in the next section.

With a given physical structure, there is but one way to get to normal operation: reduction of V_D. In view of Fig. 3b, V_D would have to be dropped to 20V to reduce M_n to less than 1.005. On the other hand, to design a structure for $\alpha < 1$ at $V_D = 100V$, the electric field in the collector depletion region must be reduced. This can be done by increasing the width of the n-epi region and reducing N_d.

The turn-on time τ can be approximated by the sum of the emitter capacitance charge-up time τ_E, the base transit time τ_B and the collector transit time τ_C.

$$\tau_E = \tau_E C_{TE} = (V_T/j)(q\epsilon N_a / V_{bi})^{1/2},\qquad(13)$$

$$\tau_B = w_B^2 / (2D_n),\qquad(14)$$

$$\tau_C = w / v_{sat},\qquad(15)$$

where V_{bi} is the built-in potential of the emitter junction, amounting to 1.0V. A V_{BE} of 0.8V results in $\tau = 1 + 60 + 70ps = 130ps$. If the plasma-filament causes local forward bias for at least this time, then initiation of second-breakdown is possible.

3. The Critical Point for Second Breakdown

The critical point for second breakdown is defined here as the operating condition of unstable equilibrium which forms the boundary between the region where the collector current increases regeneratively to the extreme values of second breakdown and the region where it regeneratively dies out to zero. The currents induced by a particle track have to at least exceed the critical point at some location in order to trigger second breakdown. The critical point depends not only on the geometry of the structure, but also on the distribution pattern of the base current. In this paper, only the simplest conceivable configuration is analyzed to gain some basic insight. To this end, the transistor structure is slightly idealized as shown in the insert of Fig 4: the neutral base layer is approximated by a flat sheet and the ground contact is approximated by a perpendicular surface of zero potential, a distance d from the edge of the base layer. The critical point is sought for the condition where the base potential varies only in y-direction, is highest at the edge, $y = 0$, and drops monotonically toward zero at the contact $y = d$. Avalanching in the channel of the MOSFET proper along the entire drain edge, as described in the introduction leads to this condition. The base current must vanish at $y = 0$. In view of Eqns. 7c, 8, and 10, the density of the avalanche hole current entering the base from the collector is

$$j_h(y) = (M_n - 1)j(y)$$
$$= (M_n - 1)[qD_n n_i^2 / (N_a w_B)] \exp[V_{BE}(y)/V_T]\quad(16)$$

The base current i_B (per unit width of the structure) and the hole current density j_h are related to V_{BE} by the differential equations

$$Ri_B(y) = -dV_{BE}(y)/dy,\qquad(17)$$

$$Rj_h(y) = Rdi_B(y)/dy = -d^2V_B(y)/dy^2.\qquad(18)$$

$$R = 1/(qN_a\mu_p w_B),\qquad(19)$$

where $R = 8.4k\Omega$ is the sheet resistance or the neutral base layer. Eqns. 17 and 18 and the conditions on V_{BE} and i_B form the boundary-value problem

$$d^2V_{BE}(y)/dy^2 = -R(M_n - 1)$$
$$[qD_n n_i^2/(N_a w_B)]\exp[V_{BE}(y)/V_T],(20a)$$

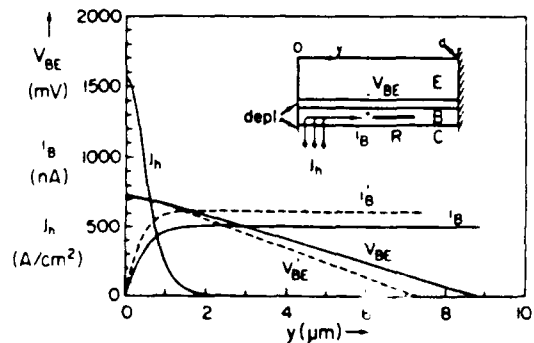$$i_B(0) = 0, \quad V_{BE}(d) = 0.\qquad(20b)$$

Figure 4: Hole current density j_h, base current i_B, and base potential V_{BE} at critical point for second breakdown. Insert: Geometry and definition of variables.

Eqn 20a is reminiscent of the equation for the electric potential on the p-side of a pn step-junction, which is

$$d^2\phi(y)/dy^2 = -(q/\epsilon)[-N_a + n_i \exp(\phi/V_T)]. \qquad (21)$$

Solutions for V_{BE} are thus expected to resemble the solutions for ϕ, which are well-known. This is borne out by Fig. 4 where V_{BE}, i_B and j_h are shown. This solution has been obtained by numerically integrating the equation from $y = 0$ and artificially putting the base contact at the point where the potential vanishes. Thus, the solution is self-consistent by fiat.

Now consider the base potential at $y = 0$ lowered by a small amount, say $10mV$. This reduces the current density by 30%, which lowers the base current and reduces the slope of the potential, which, in turn, lowers the potential at $y = 0$ some more: a regenerative feedback loop to quickly reduce currents and potential to zero sets in. Conversely, if the potential at $y = 0$ is raised by a small amount, the current density is raised exponentially, the base current and the slope of the potential become larger (dashed curves in Fig. 4), which raises the potential at $y = 0$ some more and regeneratively increases currents and potential until high-level injection and other effects reduce M_n and beta of the transistor. Heating then leads to burnout.

To make the structure less vulnerable to second breakdown, one needs to raise the critical point to higher base voltages and collector currents. This can be achieved by reducing M_n, d and R and by increasing N_a and w_B.

4. Evolution of the Plasma-filament

The evolution of the plasma-filament is governed by: (1) the kinetic energy of the heavy ion and its stopping power in silicon; (2) the impurity profiles of the transistor structure; and (3) the diffusion coefficients and mobilities of the carriers in the filament. Ziegler [7] has compiled comprehensive data on stopping power as a function of ion energy, ion species and stopping material. To first order, stopping power is proportional to the square of the charge of the ion and inversely proportional to its kinetic energy [8]. The stopping power determines the number of ehp generated per unit track length, while the kinetic energy determines the time-of-flight through the structure.

For instance, the stopping power in Si is $6.3MeV/\mu m$ for a $150MeV$ Fe ion, and $0.16MeV/\mu m$ for a $4MeV$ alpha-particle. The corresponding times-of-flight through the $10\mu m$ thick active transistor region are 0.5 and 0.7ps, respectively. The energy per ehp is independent of the stopping power and equals $3.6eV$ [9], yielding $N_r = 1.75 \times 10^6$ and 4.4×10^4 ehp/μm, of track length for the two ions. To obtain an analytically tractable model for the evolution of the plasma-filament, the ehp profile is approximated as starting from a line source of uniform strength at $t = 0$, and diffusing radially with constant diffusion coefficient $D = kT(\mu_n + \mu_p)/2q \sim 20cm^2/s$ [10]. It is further assumed that the radial and axial motion of the carriers are completely decoupled and can be treated independently. Then, the radial profiles of electrons, n_p, and holes p_p, evolve as [11]

$$n_p(r,t) = p_p(r,t) = N_r/(4\pi Dt) \exp[-r^2/(4Dt)]. \qquad (22)$$

In the high-concentration core region of the plasma-filament, the electron and hole distributions are almost precisely congruent because the space charge associated with any deviations would cause high electric fields that would immediately disperse the charge. In other words, the electron distribution is totally screened by the hole distribution and vice versa. Potential differences between the core of the plasma-filament and the outside,

are supported by radial deviations of the hole and electron profiles in the fringe region of the filament which generate the electric fields necessary to support the radial potential differences. The peak plasma-concentration at $r = 0$, the radius r_b, where the plasma-concentration equals N_a, and the radius r_c, where it equals N_d, are plotted versus time in Fig. 5 for the Fe ion track. The figure for the alpha particle track looks almost identical, if the time scales are stretched by appropriate factors. The radius r_b approximately delimits the inner core region, where the plasma dominates conditions everywhere between collector and emitter, and where current flows directly from n$^+$-collector to n$^+$-emitter, totally overpowering the npn-structure. The outer core region, where the plasma determines the conditions only in the n-epi region, and where the transistor is active lies between r_b and r_c. The radius r_c approximately separates the outer core region from the fringe region, where the conditions are increasingly determined by the transistor structure. The radii are given by the equation

$$r_i = \{4Dt \cdot \ln(4\pi Dt N_{BC_i}/N_r)\}^{1/2}, \qquad (23)$$

N_{BC_i} denoting the background impurity concentrations, $10^{17}cm^{-3}$ for $i = b$ and $3 \times 10^{15}cm^{-3}$ for $i = c$. As shown in Fig. 5, the radii first grow to a maximum and then shrink to zero, while the peak plasma-concentration falls to N_{BC}. Integration of Eqn. 23 from 0 to r_i yields the number of ehp per unit filament length in the respective core region,

$$N(r_i) = N_P\{1 - \exp[-r_i^2/(4Dt)]\} = N_P - 4\pi Dt N_{BC_i} \qquad (24)$$

$N(r_i)$ decreases linearly with time, i.e., the rate of electrons and holes crossing the surface $r = r_i$ is constant. (The crossing is partly due to the motion of the carriers and partly due to the time variation of r_i.)

The time T_i, at which r_i just vanishes is found from Eqn. 25.

$$T_i = N_P/(4\pi D N_{BC_i}). \qquad (25)$$

The times T_b and T_c respectively amount to 0.70ns and 23ns for the Fe ion track and to 18ps and 580ps for the alpha particle track. The time T_{im} at which r_i reaches its maximum r_{im}, and r_{im} itself are

$$T_{im} = N_P/(4\pi e D N_{BC}) = T_i/e; \qquad (26)$$

$$r_{im} = [N_P/(\pi e N_{BC})]^{1/2}. \qquad (27)$$

The radii r_{bm} and r_{cm} respectively amount to $2.0\mu m$ and $8.2\mu m$ for the Fe ion track and to $0.32\mu m$ and $1.3\mu m$ for the alpha
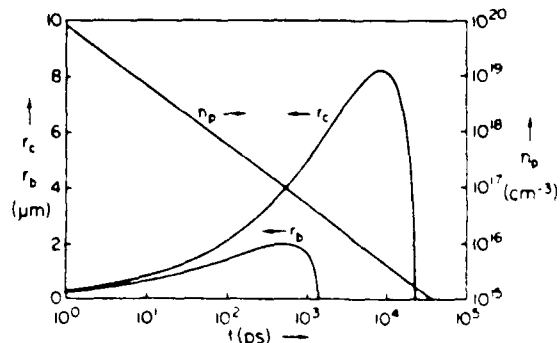
Figure 5: Radii of the core regions and central carrier-concentration of the plasma-filament from a 150 MeV Fe ion.

particle track. Finally, the fraction of the plasma carriers still inside the cylinder of radius r_{1m} is $N(r_{1m}, T_{1m})/N_p = 1 - e^{-1} = 63\%$. Eqns. 24 to 27, appeal by their simplicity.

5. Current Through the Plasma-filament

As the ion is blazing the plasma-filament into the region between the n^+-source and n^+-drain, the low resistance in its wake shorts out the potential differences, leading to a funnel-like pattern of the equipotential lines. When the conducting path between source and drain is complete, current starts to flow, with the electrons moving toward the drain and the holes toward the source while still maintaining charge neutrality. But, since the n^+-drain cannot supply holes to the filament. a negative space charge layer immediately builds up at the n-n^+ epi-substrate interface, until the resulting electric field causes avalanche breakdown. With the available electron concentrations, a local dipole-layer a few nm thick, and a potential difference of a few volts suffice to ionize one ehp per primary electron and sustain the hole current. Thus, the model of the plasma-filament is a Zener diode at the collector end in series with a resistance to the emitter of the parasitic npn transistor. The effects of this avalanche region are neglected in what follows.

The electric field in the core of the filament is constant, given by

$$E_c = V_D/|w_n + w_p|, \tag{28}$$

w_p being the metallurgical base width. The distance $w_n + w_p = 10\mu m$ results in $E_c = 100kV/cm$, which causes electrons and holes to drift with saturation velocity [12]. Consequently, the current I_1 in the core of radius r_1 is given by the product of the saturation velocity, $v_{sat} \simeq 10^7 cm/s$ for both. electrons and holes [12], and the charge per unit length of core,

$$I_1 = 2v_{sat}qN(r_1). \tag{29}$$

At $t = 1ps$, it amounts to $56mA$ for the Fe ion and to $1.3mA$ for the alpha-particle. At this early time almost the entire current flows inside the inner core directly between n^+-drain and $n+$-source. In view of Eqns. 24 and 29, the current decreases linearly with time, the current inside r_b vanishing at $t = T_b$ and that inside r_c vanishing at T_c.

Finally, a word is in order on the speed with which electric field patterns inside the plasma-filament can change. Applying skin effect theory to the plasma. penetration times of the order of $10fs$ or less are estimated. Hence, the reaction of the plasma-filament to changes of the applied fields is practically instantaneous.

6. Turn-on of the Parasitic Transistor into Second Breakdown

To induce second breakdown in the power MOSFET, the plasma-filament must locally turn on the parasitic npn-transistor beyond the critical point. To this end, the hole current that enters the neutral base layer from the filament and spreads toward the body contact must generate a sufficient local base voltage. As mentioned earlier, the critical base voltage depends on the location and on the spreading pattern of the current. Because the underlying boundary value problems are so strongly nonlinear, numerical methods to solve them inevitably have to be resorted to and need to be developed. One can, however, assess the likelihood of second breakdown reasonably well by determining the base potential distribution due to only the hole spreading current from the plasma-filament, which is an independent source. As the base layer can be approximated as a linear medium, this leads to linear boundary-value problems.

The base layer is an RC structure and therefore the spreading currents and voltages are basically governed by a diffusion equation. The applicable diffusion coefficient is given by $D_{el} = 1/(RC)$, where R is the sheet resistance of the neutral p-region and where C is the base-emitter capacitance per unit area, given by

$$C = \epsilon/w_{de}, \tag{30}$$

with w_{de} the emitter depletion layer width. For zero bias one obtains $C = 0.38 fF/\mu m^2$ and $D_{el} = 3200 cm^2 s$, the latter being two orders of magnitude larger than the carrier diffusion coefficient D. As the radial evolution of the filament is controlled by D, the spreading current and voltage are determined mainly by the sheet resistance, while the capacitance stores an insignificant fraction of the spreading charge. Consequently, the spreading process can be described approximately by Poisson's equation, which makes the problem analytically tractable.

The boundary value problem is defined by the geometry in Fig. 4 and Eqns. 20b. The top view of the geometry is sketched and pertinent parameters are defined in Fig. 6a. An image solution with an infinite number of sources and sinks as sketched in Fig. 6b suggests itself. The potential is mainly determined by the primary source and the immediately adjacent images, with more remote images loosing influence proportionally with their distances. Their main effect is a distortion of the circular equipotential lines of the primary source and a shift of the entire pattern away from the body contact.

The hole current entering the base results from (1) the holes that diffuse through the cylinder surface $r = r_b$ into the neutral base layer, (2) the hole component of the collector current in the outer core region and (3) the holes that exit through the cylinder surface $r = r_c$ into the collector depletion region and are then swept to the base by the electric field. The inner core current flows strictly between collector and emitter and does not contribute to the base spreading current.

Ignoring the current components (1) and (3). the source distribution is confined within the circle of (varying) radius r_s. Outside this radius the potential declines logarithmically, and vanishes at $r = f$. To achieve tractability for hole current component (2). the source distribution in the annular region between r_b and r_c is approximated by its average. In view of Eqn. 24.

$$p_{pav} = |N(r_c) - N(r_b)|/4\pi(r_c^2 - r_b^2)$$
$$= Dt(N_a - N_d)/(r_c^2 - r_b^2). \tag{31}$$

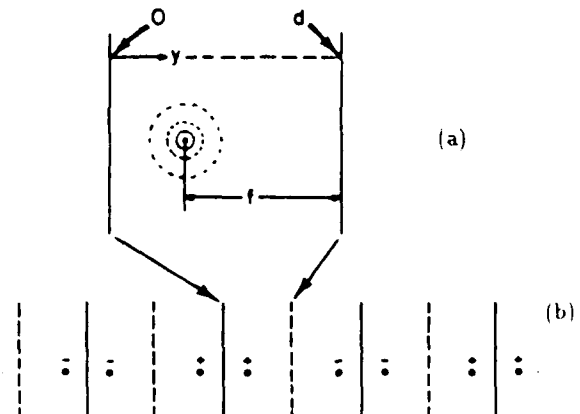Multiplying with qv_{sat} and integrating from r_b outward yields the current

Figure 6: Boundary-value problem for plasma-filament. (a) Geometry. (b) Array of images for image solution.

$$\iota_B(r) \quad \pi q v_{sat} Dt N_a (r^2 - r_t^2) \cdot (r_c^2 - r_t^2): \quad rb \cdot r \leq rc. \quad (32)$$

The element of voltage drop is the product of the current with the resistance element. and integrates to

$$V_{BE}(r_c) = (q v_{sat} Dt N_a R \cdot 2) \ln(f \cdot r_c): \quad (33)$$

$$V_{BE}(r_b) = (q v_{sat} Dt N_a R \cdot 4)(1 + 2\ln(f \cdot r_c)$$
$$- r_t^2 \ln(r_c \cdot r_b), (r_c^2 - r_b^2) \quad (34)$$

$$V_{BE}(T_b; r_b = 0) = V_{BE}(r_c)$$
$$+ (q v_{sat} Dt N_a R \cdot 4)(1 - 2\ln(f \cdot r_c). \quad (35)$$

With $f = 8\mu m$. Eqn. 35 assumes a value of 8.6V for the Fe ion track and of 0.66V for the alpha-particle. There is no doubt that the former induces second breakdown, but the latter may indeed not. The numbers should not be taken too literally, because the potentials of the image sources have not been considered and the accuracy of the approximations has not been established. The Eqn. 34 should, however, reasonably describe the behavior of $V_{BE}(r_b)$: one notices that it reaches a maximum at time T_b, when r_t just vanishes. For times beyond that point. Eqns. 31 to 35 are no longer valid in their present form. They must be rederived with the factor N_a in Eqn. 31 replaced by $p_p(0, t)$, which causes $V_{BE}(r = 0)$ to decline when $t > T_b$.

7. Discussion and Conclusions

The analyses in this paper demonstrate that significant insight into the triggering mechanism for second breakdown and single event burnout can be gained by analytical techniques. In particular, they show that the power MOSFET structure used as an example is highly vulnerable to radiation-induced burnout.

The main results stem from the analysis of the avalanche process in the parasitic npn-structure, from the estimation of the critical point for second breakdown, and from the assessment of the potential distribution generated in the base layer by the plasma-filament. The major conclusion to be drawn is certainly that the electric field intensity in the lowly doped drain epi region is the overriding contributor to burnout sensitivity. Reduction of the avalanche multiplication factor in the collector of the parasitic npn-structure is the most effective measure to increase the resistance against second breakdown.

From the user's point-of-view, the vulnerability of a power MOSFET to single event burnout can only be reduced by lowering the peak drain operating voltage. The intrinsically safe operating region for particular transistors can be assessed from measurements of burnout cross-section versus drain voltage with highly energetic heavy ions. It would be desirable to have the intrinsic threshold of the drain voltage for single event burnout specified as one of the transistor parameters.

From the device designer's point-of-view, resistance to single event burnout can be increased foremost by structural changes that, for a given drain voltage, lead to a reduction of the maximum electric field in the drain depletion region. Secondly, the resistance of the p-layer and its dimension from the MOSFET proper to the body contact (distance d in Figs. 4 and 6) should be made as small as possible. Small test transistors with the p$^-$-plug omitted could be used for a manufacturing test to monitor and guarantee the intrinsic single event burnout threshold of the drain voltage.

To model the mechanisms more accurately, numerical calculations are inescapable. In particular, two-dimensional modeling and simulation of the plasma-filament in cylindrical coordinates. or full three-dimensional simulation needs to be pursued. The transport models must include algorithms for velocity saturation and avalanche ionization. Difficulties with these simulations can be expected because of the innate instabilities of the processes, which are bound to interfere with the convergence of numerical computations.

The value of the analytical models lies less in their accuracy than in the explicit functional relationships between the variables, which show the relative influence of the individual parameters on the vulnerability to second breakdown and single event burnout.

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II.D Features of the Triggering Mechanism for Single-Event Burnout of Power MOSFETs

FEATURES OF THE TRIGGERING MECHANISM FOR
SINGLE EVENT BURNOUT OF POWER MOSFETS*

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ABSTRACT

The feedback mechanism leading to second breakdown and burnout in a power MOSFET is reviewed briefly, and critical device design parameters are identified and chosen with regard to electrical specifications. Based on typical parameters, the avalanching conditions in the space charge region of the collector junction are investigated over a wide range of collector current densities. It is shown that the space charge associated with the collector current density modifies the electric field profile such that, with increasing collector current, the avalanche multiplication factor rises to a peak, then declines to a valley, and eventually rises monotonically. This behavior can be explained in simple terms. It may lead to a stable avalanching condition with a current density too low to damage the structure. This condition can be initiated by heavy ions with energies below a certain threshold. Ion energies beyond the threshold drive the avalanching process into the region of monotonic increase of the avalanche multiplication factor and lead to run-away and burnout. The threshold for runaway varies widely with changing configurations of the p^+-plug and of the p-body region and promises configurations that are immune to burnout. Assessments of threshold currents in a typical hex cell are given.

1. INTRODUCTION

Power MOSFETS are vulnerable to single event burnout induced by energetic heavy ions. The sequence of processes leading to the failure of the transistor is initiated by the plasma filament generated by the passage of a heavy ion. Electrons flow through the filament from the source n^+-region to the substrate n^+-region, while holes flow out of the plasma filament through the body p-region to the body contact. When the filament is located near the channel of the MOSFET, as shown in Fig. 1, the voltage drop generated by the hole current along the p-region tends to forward-bias the junction between the p-region and the source. This forward-bias is highest near the filament and there it most strongly turns on the parasitic bipolar npn transistor indicated in Fig. 1. Usual operating voltages of the power MOSFET maintain sufficient electric fields in the collector depletion region to cause significant avalanche multiplication. Thus, every electron entering the collector depletion region from the base causes one or more holes to return to the base, enhancing the
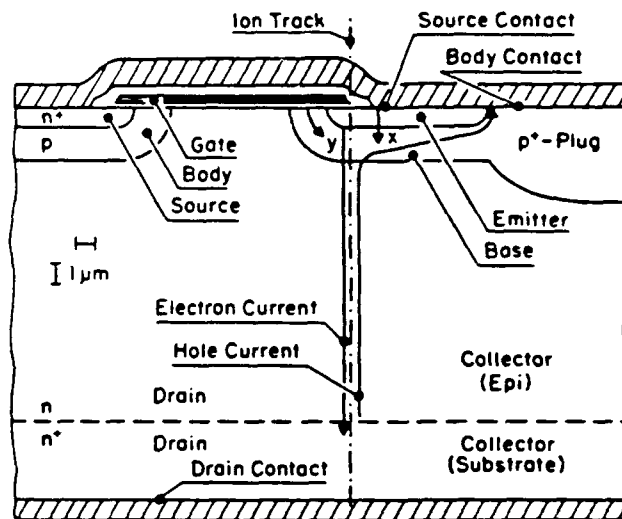

Fig. 1. Power MOSFET structure.

current and the voltage drop along the body layer [1]. This regenerative effect rapidly increases the collector current to high values, driving the npn transistor toward second breakdown. Phenomenologically, second breakdown is the sudden collapse of the collector-emitter impedance of a bipolar transistor operated under high voltage and current, typically with ensuing irreversible failure [2].

The characteristics of the feedback process are mainly determined by the current gain of the parasitic npn transistor, by the resistance of the p-body region between the MOSFET channel and the body contact, and by the avalanche multiplication in the collector depletion region [1]. Avalanche multiplication is strongly dependent on the width and doping level of the n-epi region. The process can be separated into four parts: (1) hole current from avalanche multiplication in the collector depletion region, (2) division of the hole current between the body region and the emitter junction, (3) voltage drops along the body region due to that part of the hole current that flows to the body contact, and (4) electron transport from the emitter to the collector through the charge-neutral base.

The device cross-section shown in Fig. 1 clearly demonstrates that the overall problem is at least two-dimensional. However, in order to improve tractability and insight, its parts are modeled in one-dimensional approximations. To this end, consider the parasitic bipolar transistor sliced into thin vertical strips (slabs, when the third dimension, in the direction of the channel width, is considered), and each strip

treated as an independent, one-dimensional transistor. The two-dimensional effects are accounted for merely by the changing emitter voltage from strip to strip.

This paper reports on the avalanching conditions in the collector depletion region in terms of the design and operating parameters of the power MOSFET and on the conditions that lead to a regenerative increase of the collector current of the parasitic npn transistor. This investigation forms a crucial part of an effort aimed at developing a complete set of models for predicting the stopping power of an ion necessary to cause single event burnout in a power MOSFET and to explicitly relate this stopping power threshold to the physical and electrical parameters of the transistor.

General derivations and arguments alone cannot provide the insight into the intricate interactions needed to predict the feedback behavior in the npn transistor that leads to the high-current conditions. Therefore, it is important to inspect particular cases in detail. To this end, and also to assess ranges of pertinent parameters, the basic relationships between electrical device characteristics and impurity levels and profiles are reviewed in Section 2. The device structure for studying the avalanche and feedback mechanisms is chosen here and all parameters are defined. In Section 3 the basic relationships between collector current, space charge distribution, electric field profile, and impact ionization in the collector depletion region are retraced. Results of numerical calculations are presented and discussed. The space charge associated with the collector current is shown to incisively modify the electric field distribution and avalanche multiplication. The consequences of this behavior are studied in Section 4, where the existence of a stable, low-power avalanching condition within a hex-cell is predicted. This harmless operating condition may have been observed experimentally by Waskiewicz et al. [3]. Section 5 contains estimates of threshold currents in a typical hex cell of a power MOSFET.

2. POWER MOSFET DESIGN PARAMETERS

This section is devoted to a review of the power MOSFET design parameters exerting the most influence on mechanisms leading to single event burnout, in order to choose the parameter values for the ensuing analysis. The physical structure of the power MOSFET is determined by the breakdown voltage required and by the desired electrical properties of the channel region. The resulting impurity profiles of the p-body and n-epi regions, in turn, control the mechanisms leading to single event burnout.

The device breakdown voltage establishes the thickness and doping level of the n-epi layer. The overall structure of the transistor and the configuration of the electric fields in the collector junction justify the approximation of the latter by a planar, highly asymmetric, or even a one-sided step junction. The reverse breakdown voltage, V_B, is related to the depletion layer width at breakdown, w_B, by [4]
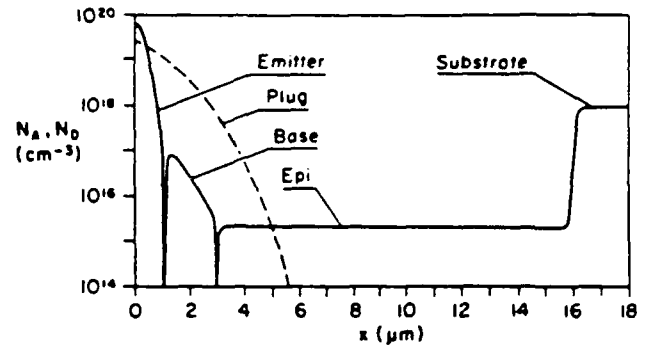

Fig. 2. Impurity profiles of $n^+ p n n^+$ structure.

$$V_B = (5.8 \times 10^4 \text{ Vcm}^{-0.84}) w_B^{0.84}, \tag{1}$$

and this leads to the epi doping level, N_D, by

$$N_D = 2\varepsilon V_B/(q w_B^2), \tag{2}$$

where ε and q denote the permittivity of silicon and the charge of the proton, respectively. In the case further considered in this paper, a depletion width, w_B, of 11 μm leads to $V_B = 190$ V and $N_D = 2 \times 10^{15} \text{ cm}^{-3}$.

The desired threshold voltage and channel length of the MOSFET proper establish the p-body impurity profile and the recess of the n^+-source diffusion from the edge of the p-diffusion. The threshold voltage, V_T, is given by [5]

$$V_T = V_{FB} + 2|\phi_p| + (T_{ox}/\varepsilon_{ox})[2\varepsilon q N_A (2|\phi_p|)]^{1/2}, \tag{3}$$

where T_{ox} is the gate oxide thickness, N_A is the highest acceptor concentration along the channel, $|\phi_p| = (kT/q)\ln(N_A/n_i)$, and V_{FB} is the flatband voltage, which equals about -0.9 V for a heavily n-doped polysilicon gate electrode. For the case considered in this paper, $T_{ox} = 100$ nm and $N_A = 3 \times 10^{17} \text{ cm}^{-3}$ result in $V_T = 8$ V. The acceptor concentration along the channel progressively declines with distance from the source. The two acceptor concentrations, $3 \times 10^{17} \text{ cm}^{-3}$ at the source junction and $2 \times 10^{15} \text{ cm}^{-3}$ at the drain junction, determine the essentially Gaussian acceptor profile of the p-body region. The profile of the p^+-plug, also essentially Gaussian, needs to provide low resistance to the body contact and a deeper drain junction to concentrate drain breakdown currents below the body contact. The profiles for the chosen parameters are shown in Fig. 2, with that of the p^+-plug indicated by a dashed line.

Considerations of photolithography and fabrication determine the horizontal dimensions of the source and p^+-plug regions. Variations of the channel length are minimized by employing self-alignment techniques for the p-body and source depositions, while the minimum recess distance of the p^+-plug is limited by mask alignment tolerances.

3. AVALANCHE EFFECTS IN THE COLLECTOR

In this section, the intimate and strongly nonlinear interactions between collector current, electric field distribution,

and avalanche multiplication in the collector depletion region are discussed, the numerical method for calculating the resulting carrier concentrations is described, and results are presented. As described earlier, a one-dimensional solution within a narrow strip along the x-coordinate shown in Fig. 1 is considered. For discussion and computation, the impurity profile of Fig. 2 is approximated by the idealized one of Fig. 3a. The space charge distribution, ρ_0, and the electric field, E_0, in the collector depletion region for 180 V reverse voltage and zero collector current density are shown in Figs. 3b and 3c by thin lines. One recalls that, by Poisson's equation, the electric field is proportional to the integral of the space charge density and, conversely, the slope of the electric field function is proportional to the space charge density. The area under the electric field function is equal to the applied voltage, V_D.

Under the given conditions, the electric field exceeds the critical field for electron velocity saturation (30 kV/cm) over most of the width of the depletion region. The hole velocity saturates only at about 200 kV/cm, and reaches 70 % of saturation velocity at 50 kV/cm. Consequently, electrons travel from x_p to X_n, or holes travel from x_n to x_p near or at their saturation velocity of 10^7cm/s over most of the distance. Approximating the actual carrier velocities by an average velocity across the entire depletion region has led to insignificant errors in avalanche breakdown calculations [4]. This approximation renders the collector current density components $j_n(x)$ and $j_p(x)$ proportional to the carrier concentrations $n(x)$ and $p(x)$ and relates them to j_C by

$$j_n(x) = -qv_{SAT}n(x); \qquad (4a)$$

$$j_p(x) = -qv_{SAT}p(x); \qquad (4b)$$

$$j_C = -qv_{SAT}[p(x)+n(x)]. \qquad (4c)$$

In one-dimensional flow, j_C must be constant because of current continuity. Now, consider a collector current with a density of 1600 A/cm² flowing through the depletion region. Such a current density would be found in a typical bipolar transistor operating at about one third of its rated current. It adds an electron concentration, $n(x)$, of 10^{15} cm⁻³ and halves the space charge density on the n-side. When collector current flows, the depletion region is no longer truly depleted. To reflect this, it will be called space charge region in what follows. The space charge density, ρ_j, and electric field, E_j, resulting from the added current are shown in Figs. 3b and 3c by heavier lines. The space charge region has grown across the entire epi layer and imperceptibly into the n⁺-substrate, and the peak electric field has been reduced by about one fourth. The edge of the space charge region, x_p, has shifted slightly to the right.

The number of electron-hole pairs generated per unit path length of a primary carrier is defined as the impact ionization rate α. Following an analysis by Sze [6], α can be approximated by [6]

$$\alpha = A\exp\text{-}(E_I/E), \qquad (5)$$

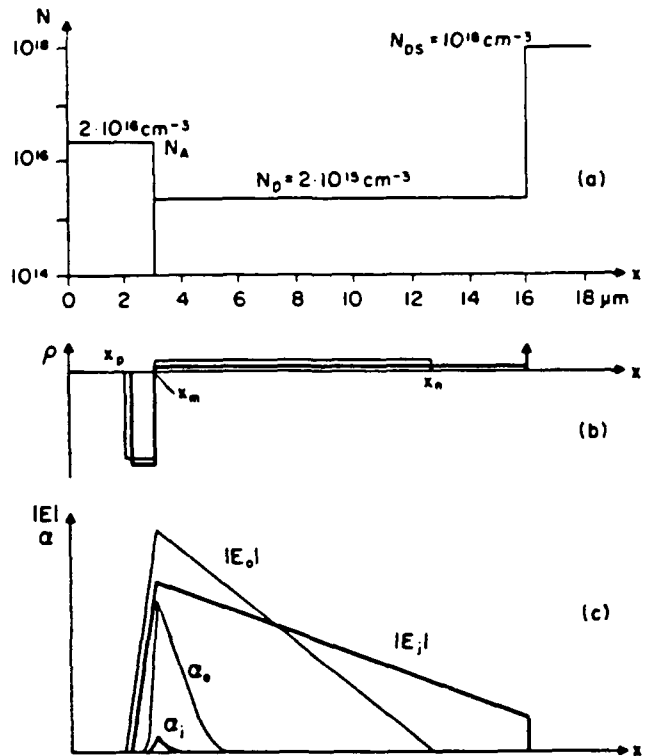

Fig. 3. (a) Approximated pnn⁺ profile for simulations. (b) Charge density in the space charge region for zero and non-zero current. (c) Electric field and ionization rate in the space charge region for zero and non-zero current.

where A and E_I, respectively, equal 89 μm⁻¹ and 1.2 MV/cm for electrons and 260 μm⁻¹ and 2.0 MV/cm for holes. Plots of the ionization rates for electrons, α_0 and α_j, resulting from the fields, E_0 and E_j, respectively, are sketched in Fig. 3c. The corresponding ionization rates for holes are much lower and are neglected here. The avalanche multiplication factor, M, is defined as the average number of holes that return to the base edge at x_p for every electron entering the space charge region from there. M grows with the area under the $\alpha(x)$-curve; for low current densities the relationship can be described analytically [1]. The large reduction of $\alpha(x)$ with rising collector current demonstrated by Figs. 3b and 3c certainly causes M to decrease rapidly. The decline continues until the electron concentration reaches that of the donors in the epi region. At that point, the space charge in the epi essentially vanishes and the electric field becomes constant. When the current rises further, the net space charge in the epi grows negative. In turn, the peak of the electric field shifts to the epi-substrate interface and rises, which now causes M to grow progressively with collector current.

To improve insight, the hole concentration at x_p has been calculated numerically as a function of the electron concentration at x_p (stemming from injection at the forward-biased emitter junction). To this end, given the impurity profile, the electron concentration at x_p and the applied drain voltage, V_D, initial profiles of space charge, $\rho(x)$, electric field, $E(x)$, potential, $V(x)$, and ionization rate, $\alpha(x)$, are calculated and stored for typically 300 points across the space charge region
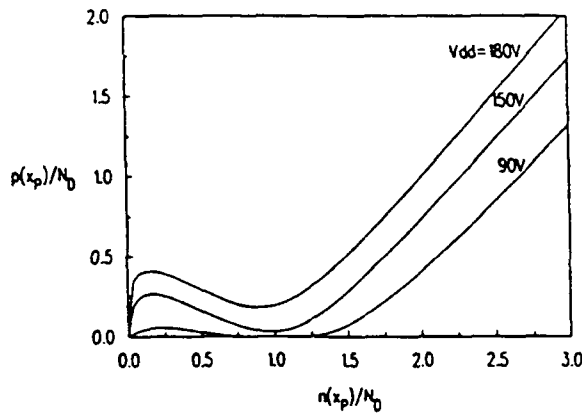
Fig. 4. Avalanche-curves: normalized hole concentration versus normalized electron concentration.
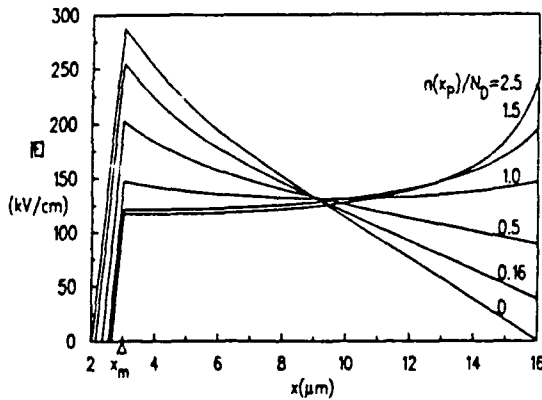

Fig. 6. Ionization rate in the space charge region.

Fig. 5. Electric field in the space charge region.

Fig. 7. Electron concentration in the space charge region.

and epi layer, using trapezoidal integration starting from x_p. From $\alpha(x)$, a revised electron concentration, $n(x)$, is calculated by integrating the equation [1]

$$dn(x)/dx = \alpha(x)n(x), \tag{6}$$

again using the trapezoidal rule. Then, $p(x)$ is calculated from $n(x)$ and Eqns. (4). These carrier concentrations are used to update the space charge profile for the next iteration step. The value x_p is updated by an algorithm to reduce the difference between the calculated $V(x_n)$ and V_D. The iteration stops when, within prescribed error margins, a self-consistent solution for the carrier densities exists simultaneously with the condition $V(x_n) = V_D$. Then, the solution is archived, the electron concentration is increased by an increment, and the iteration toward self-consistency is resumed, with the just archived solution as the initial guess.

Results are illustrated by Figs. 4 to 8; Fig. 4 showing avalanching characteristics for various values of V_D in the form of curves of the normalized concentrations $p(x_p)/N_D$ vs. $n(x_p)/N_D$, henceforth called avalanche curves. Profiles of $E(x)$, $\alpha(x)$, $n(x)$ and $p(x)$ are shown in Figs. 5 to 8 for operating conditions along the avalanche curve for $V_D = 180$ V. The curves of Fig. 4 bear out the decrease of M with increasing electron concentration; in fact, a region exists where not only $M = p(x_p)/n(x_p)$, but even $p(x_p)$ decreases. In this region, in-
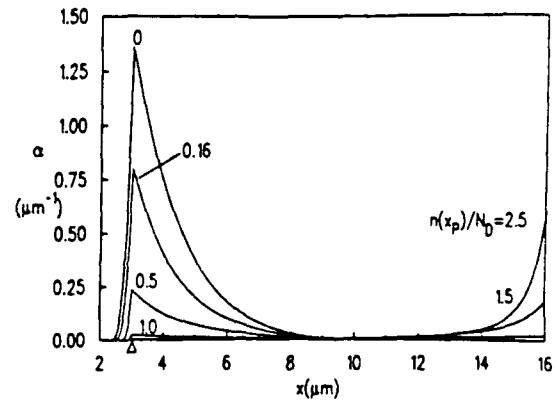
creasing electron current from the emitter leads to decreasing avalanche hole current. The minimum of $p(x_p)$ occurs near the point $n(x_p) = N_D$, indicated by the abscissa 1 in Fig. 4. The second rising branch of the avalanche curve approaches an asymptote with a slope close to unity. The asymptote shifts to the right as V_D and, hence, the depletion width for zero current decrease. This also makes the valley deeper.
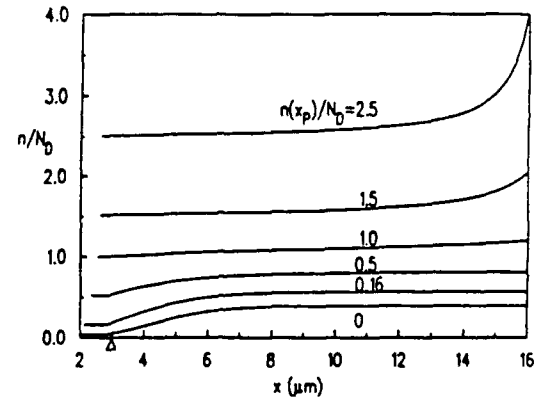
The more the epi layer width exceeds the space charge layer width for zero current density, the deeper and wider the valley in the avalanche curve becomes, and the more its final rising branch moves to the right. The valley can be widened and deepened either by reducing the operating voltage, as done to create Fig. 4, or by increasing the epi layer thickness.

The electric field profiles of Fig. 5 behave in principle as discussed earlier. The variation of the peak and its shift from the metallurgical junction to the epi-substrate interface occur as expected. The varying charge density across the space charge region due to impact ionization, which was ignored in Fig. 3, causes the profiles to be curved rather than composed of straight line segments. Fig. 6 demonstrates the high sensitivity of α to E. Finally, Figs. 7 and 8 show the electron and hole concentrations across the space charge region.

The curves for the two highest electron concentrations in each of these displays hold the key to understanding the asymptotic behavior of the avalanche curve. This insight is
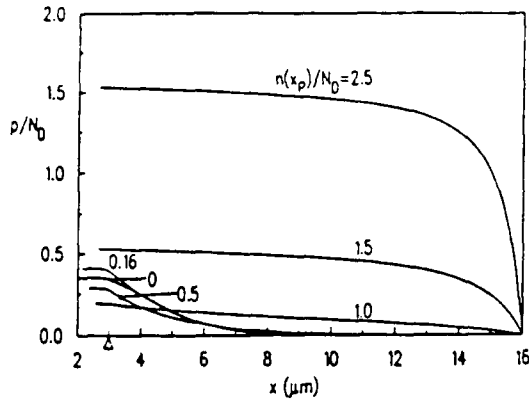
Fig. 8. Hole concentration in the space charge region.

Fig. 9. Model of the parasitic, bipolar npn structure.

crucial because the regenerative feedback conditions involve operation of the collector junction at high current densities for which numerical simulation becomes extremely inefficient or impossible. Starting with the E-curves, one notes that the two significantly different electron concentrations lead to almost identical electric fields over most of the space charge region, suggesting that the space charge densities must also be nearly the same. The deviations are largest near the epi-substrate interface, where the fields are highest and have the most influence on α, and where most of the hole generation occurs. The electron and hole concentrations are essentially constant across much of the space charge region and equal to $n(x_p)$ and $p(x_p)$, respectively. The concentration $p(x_p)$ is proportional to the generation activity at the epi-substrate interface. Now, as $n(x_p)$ rises, the electric field at the epi-substrate interface tends to rise and raises the generation and concentration of holes just enough to maintain the charge density in the space charge region essentially unchanged. Hence, once $n(x_p)$ is sufficiently larger than N_D, the hole concentration, $p(x_p)$, must rise at essentially the same rate as the electron concentration, $n(x_p)$, giving the avalanche curve nearly unity slope.

In this case, the extreme sensitivity of α on E maintains the field distribution and the location of x_p almost the same, even for very high electron concentrations. At low drain voltages, e.g., $V_D = V_B/2$, where the linearly rising branch of the avalanche curve is shifted to significantly higher electron concentrations, the left edge of the space charge region recedes somewhat into the epi region, an effect known as base push-out.

4. THRESHOLDS FOR REGENERATION

To investigate the regenerative feedback process, the geometry of the parasitic npn structure consisting of the body region and adjacent features is approximated by that shown in Fig. 9, where the essential variables are also indicated. The complication introduced by the p^+-plug is dispensed with by considering two extreme cases, one where the plug region is recessed to the far end of the source contact as shown in Fig 1, and the other where the plug region extends nearly to the
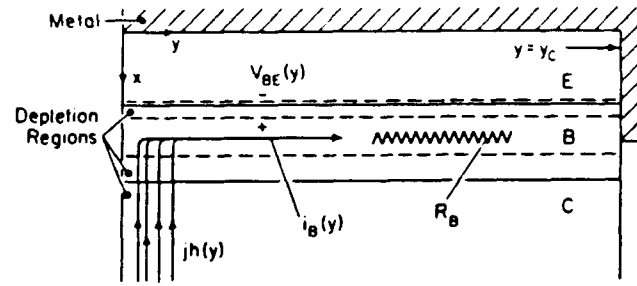
channel edge of the source region. In terms of the model, the only difference between the two cases is the value of the sheet resistance of the charge-neutral p-layer.

The conditions for regenerative feedback have been described and investigated elsewhere [1] under the assumption of current-independent avalanche multiplication, i.e., by neglecting the effects of the space charge associated with the collector current. Under this assumption, the existence of a threshold, distinguished by an (unstable) equilibrium condition of the feedback mechanism, has been proven and identified by particular values of V_{BE}, j_p, $p(x_p)$, etc., at $y = 0$. The threshold is basically given by the amount of hole current needed to generate the voltage drop along the body region to forward bias the parasitic npn structure just right. If this threshold is minutely exceeded, regenerative feedback sets in and drives the operating point to ever increasing currents, while any excitation not reaching the threshold decays to zero.

In Fig. 4, current-independent multiplication would be represented by the tangents to the avalanche curves at the origin; obviously an approximation that rapidly becomes unrealistic as the electron concentration increases. The valley in these curves suggests that a stable equilibrium condition may exist, characterized by a point, $n_2(x_p), p_2(x_p)$, on the declining branch. When this is the case, the feedback process causes the operating point to coast toward this point from any initial condition identified by a value of $n(x_p, y=0)$ in a neighborhood of $n_2(x_p)$. This occurs either from below, with regeneratively increasing emitter current, or from above, with decaying emitter current. The neighborhood is bounded by a lower unstable equilibrium condition or threshold, $n_1(x_p), p_1(x_p)$, and an upper one, $n_3(x_p), p_3(x_p)$. Initial conditions below the lower threshold decay with time to zero, while initial conditions above the upper threshold lead to regenerative runaway toward high currents and burnout.

Returning to the model of Fig. 9, one finds the feedback process formally governed by the same second order differential equation in V_{BE} and boundary conditions as for a constant multiplication factor [1],

$$d^2V_{BE}/dy^2 = -MR[qD_n n_i^2/(N_A w)]exp[V_{BE}/V_T], \quad (7a)$$
$$Ri_B(0) = -dV_{BE}(0)/dy = 0, \quad V_{BE}(y_C) = 0. \quad (7b)$$

However, M is no longer a constant, but a function of the electron concentration, derived from the curves of Fig. 4 by the relation $M = p(x_p)/n(x_p)$. In Eqn. (7a), R is the sheet re-

sistance of the neutral p-body region, D_n is the electron diffusion constant in the base region, N_A is the average hole concentration in the base region, w is the width of the neutral base, V_T stands for kT/q and y_C is the location of the body contact, as indicated in Fig. 9. The electron concentration $n(x_p)$, the hole concentration, $p(x_p)$, and the hole current density, $j_p(x_p)$, are given by the equations

$$n(x_p) = [D_n n_i^2/(N_A w v_{SAT})]exp(V_{BE}/V_T), \qquad (8)$$

$$j_p(x_p) = q v_{SAT} p(x_p) = q v_{SAT} M n(x_p). \qquad (9)$$

Dividing Eqn. (7a) by R makes its left side equal to the local hole current density, given as the derivative of the body current with respect to y. The latter is the derivative of V_{BE}/R with respect to y. The right side is the product of M(y) with the local emitter current density. In view of the high beta of the npn transistor, the hole current component flowing through the emitter junction is small compared to that flowing along the body layer and is neglected.

To explore conditions, Eqn. (7a) can be integrated numerically from the left, choosing an initial value $V_{BE}(0)$. Such a simulation leads to a profile of $V_{BE}(y)$. If the correct value for $V_{BE}(0)$ is chosen, $V_{BE}(y)$ vanishes precisely at $y = y_C$. It is instructive to also inspect the functions $j_p(x_p,y)$ and $i_B(y)$. Results of such simulations for the case with the p$^+$-plug recessed as in Fig. 1 are displayed in Fig. 10. The parameters used for the calculation are $R = 5$ kΩ, $D_a = 23$ cm^2/s, $N_A = 2 \times 10^{16}$ cm^{-3}, w = 0.75 μm, $y_C = 8$ μm and $V_D = 180$ V. The profiles of $j_p(x_p,y)$, $i_B(y)$ and $V_{BE}(y)$ are shown for the three initial values of $V_{BE}(0)$ for which the boundary condition $V_{BE}(y_C) = 0$ is satisfied. These are the three equilibrium conditions possible for this case; the outer ones unstable, the center one stable. The three values of $V_{BE}(0)$ are 745 mV, 755 mV and 766.5 mV. They lead to values for $n(x_p,0)$ of, respectively, 0.85×10^{15} cm^{-3}, 1.25×10^{15} cm^{-3} and 1.95×10^{15} cm^{-3}, and place the first two operating points on the declining branch of the avalanche curve for 180 V, while the third is located barely beyond the minimum.

A few observations are in order at this point. The existence of three equilibrium conditions is precarious in this case; further simulations showed that they occur only if y_C falls within a region less than 0.1 μm wide. For smaller y_C, only the upper threshold remains and shifts toward higher $n(x_p,0)$, and vice versa for larger y_C. The three equilibrium points would be spread wider if the avalanche curve had a deeper valley. Either a thicker epi layer or a lower drain voltage would achieve this by shifting the second rising branch to the right.

The hole currents are concentrated within about the first 3 μm in y. The areas under the j_p-curves determine the final base currents which, in turn, establish the final slope of the V_{BE}-curves. The three base currents are of similar magnitude, approximately 22 μA per μm of channel width. The electron concentrations are largest at the edge $y = 0$ and decay
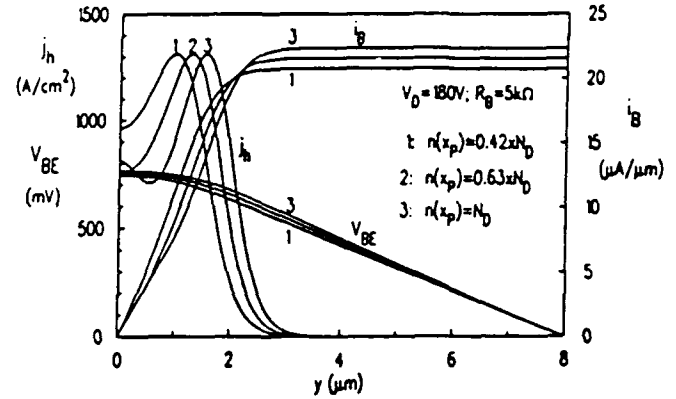

Fig. 10. Hole current densities j_h, base currents i_B and base potentials V_{BE} at the three equilibrium conditions of the model with recessed p$^+$-plug.
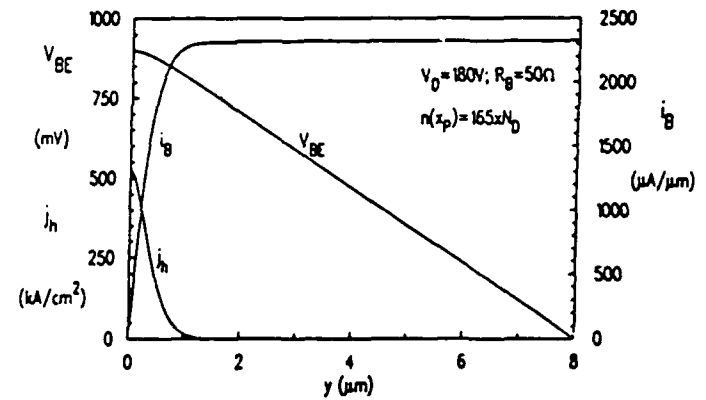

Fig. 11. Hole current density j_h, base current i_B, and potential V_{BE} at the equilibrium condition of the model with expanded p$^+$-plug.

monotonically with increasing y. The same is true for the collector current densities $j_n(y)$ which, at $y = 0$, reach significantly different values of 950 A/cm^2, 720 A/cm^2 and 616 A/cm^2, respectively.

The other extreme case, where the p$^+$-plug extends to the edge of the p-body, is characterized by a base sheet resistance about two orders of magnitude lower. It is only cursorily explored here by repeating the simulation with $R = 50$ Ω and all other parameters unchanged. For this computation, the avalanche curve is extrapolated to higher electron concentrations by a straight line of unity slope. It leads to the profiles displayed in Fig. 11, and to $n(x_p,0) = p(x_p,0) = 3.3 \times 10^{17}$ cm^{-3} and $j_n(0) = j_p(0) = 5 \times 10^5$ A/cm^2. This operating point is far beyond the range displayed in Fig. 4 and exceeds the current capabilities of the npn transistor by some two orders of magnitude, making the result unrealistic. In reality, the threshold current for regenerative runaway can never be reached in this case, and the disturbance from any heavy ion simply dies out. The device is immune to single event burnout. The curves in Fig. 11 have the same characteristics as those obtained in a simulation based on a constant multiplication factor [1]. This is not surprising; for electron concentrations in the space charge region much larger than N_D, the multiplication factor indeed approaches a constant, namely unity, as borne out by Fig. 4.

5. DISCUSSION AND CONCLUSIONS

In the preceding two sections, the relationships between the concentration of electrons constituting the collector current and the hole concentration generated by these electrons have been explored by numerical computations based on a representative set of parameters. Some basic characteristics of these relationships have been discussed. The results have been applied to a simplified model for the feedback mechanism in the parasitic npn transistor of a power MOSFET. Threshold conditions for onset of regenerative runaway of currents have been explored for two device structures that differ in the amount by which the p^+-plug is recessed from the edge of the p-body region.

Since results are cast mainly in terms of carrier concentrations and current densities, it is of interest to convert them to currents in a power MOSFET. To this end, consider the dimensions of Fig. 1 applied to a hex cell with an edge-to-edge dimension of the p-body region of 30 μm. The resulting perimeter of about 100 μm constitutes the channel width for the cell. In a hex cell with these dimensions and with recessed p^+-plug, the three conditions displayed in Fig. 10 generate very similar base currents of 2.0 mA, 2.1 mA and 2.2 mA, but distinctly different collector currents of 1.2 mA, 2.0 mA and 3.5 mA. For the hex-cell with the p^+-plug extended to the border of the body region, the threshold for regenerative runaway of the currents lies beyond the capabilities of the npn transistor, such that the triggering mechanism is disabled.

These estimates indicate that the expansion of the p^+-plug region is a very effective method for raising the threshold for regenerative runaway of the currents toward second breakdown and burnout. Since the npn transistor cannot support the threshold currents of the device structure with extended p^+-plug, it appears plausible that power MOSFETs can be designed to be immune to single event burnout, even when they are operated close to their breakdown voltage. The successful computation of avalanche curves for a wide range of conditions forms the basis for modeling the avalanching behavior by analytic approximations.

6. ACKNOWLEDGEMENTS

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II.E Temperature Dependence of Single-Event Burnout in *N*-Channel Power MOSFETs

TEMPERATURE DEPENDENCE OF SINGLE-EVENT BURNOUT IN N-CHANNEL POWER MOSFETs [†]

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ABSTRACT

The temperature dependence of single-event burn out (SEB) in n-channel power metal-oxide-semiconductor field effect transistors (MOSFETs) is investigated experimentally and analytically. Experimental data are presented which indicate that the SEB susceptibility of the power MOSFET decreases with increasing temperature. A previously reported analytical model that describes the SEB mechanism is updated to include temperature variations. This model is shown to agree with the experimental trends.

I. INTRODUCTION

It has been known for some time that single-event burnout (SEB) of power metal-oxide-semiconductor field effect transistors (MOSFETs) is a catastrophic failure mode that can be triggered by the passage of a single heavy ion through the device [1]. This phenomenon is of concern to space-born system designers since heavy ions are ubiquitous in the space-radiation environment [2]. In addition, the broad range of temperatures that may occur on board a system in flight necessitates an investigation of the temperature dependence of the SEB mechanism.

Power MOSFET burnout has been attributed to the turn-on of the parasitic bipolar-junction transistor (BJT), inherent to the double-diffused metal oxide semiconductor (DMOS) structure, when the power MOSFET is turned off (blocking a large drain-source bias) [3]. Previous burnout modeling has been performed for an ambient device temperature of 300 K. This paper reports the temperature dependence of the burnout mechanism in n-channel power DMOS devices.

Observation of SEB in p-channel power MOSFETs has not been reported in the literature. It is believed that the much lower impact-ionization rate for holes than electrons is responsible for the apparent hardness to SEB seen in p-channel power MOSFETs [3]. For this reason, the temperature dependence of SEB in p-channel devices will not be presented in this paper.

The non-destructive burnout experiment method, with a means to control the ambient temperature of the device, was performed on IR6766 and IRF150 power MOSFETs. The SEB cross-section was measured as a function of drain-source voltage and temperature. The temperature was varied from 300 K to 373 K. Due to the difficulty (or impossibility) of cooling devices within the experimental chamber, only temperatures at and above room temperature are investigated herein. The experimental results indicate that the burnout susceptibility of a given device decreases with increasing temperature for a given applied drain-source voltage.

The details of the testing technique are given in Section II. The experimental results are presented in Section III. The burnout mechanism for the power DMOS device structure is reviewed, and the temperature dependence of the model is discussed in Section IV. The temperature dependence of the SEB threshold is then calculated for a typical DMOS device in Section V. Finally, conclusions are given in Section VI.
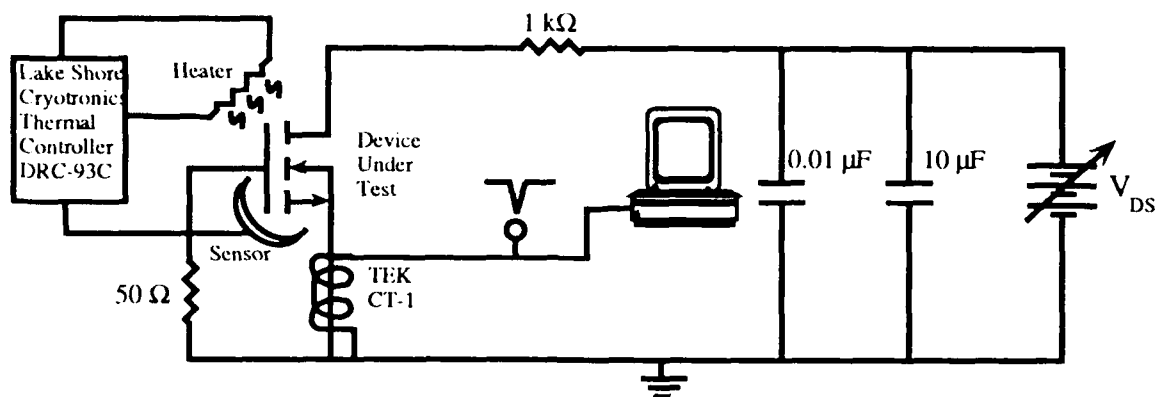
Figure 1: Non-destructive, temperature controlled SEB test set-up.

II. BURNOUT EXPERIMENT

The IR6766 and IRF150 n-channel power MOSFETs with breakdown voltages, BV_{DS}, of 200 V and 150 V, respectively, were subjected to heavy ion bombardment in the 88-inch cyclotron facility at Lawrence Berkeley Laboratories. A monoenergetic beam of 380 MeV Kr ions at a fixed LET of 41 MeV-cm²/mg was used to characterize the devices. The devices were de-lidded prior to heavy ion exposure. Each test was performed until a total fluence of 10^7 ions/cm² was obtained, or an error of ~ 100 pulses were counted.

The ambient device temperature was maintained using the Lakshore Thermal Controller DRC-93C. The temperature controller consisted of a resistive heater and thermal sensors connected in a feedback loop. The heater and sensors were attached directly to the TO-240 package of the device under test, (DUT). It was determined that if the temperature was allowed to equilibrate for several minutes, the temperature was very uniform across the surface of the chip. This provided a reliable indication of the device temperature.

The non-destructive burnout test method was used in order to obtain SEB cross-sections for a given device type [4, 5]. The non-destructive test technique employs a current limiting resistor in the drain lead of the DUT so that the drain-source current can not rise sufficiently to induce second breakdown of the parasitic bipolar transistor and consequently burnout. The current-limited pulses were monitored at the drain terminal of the DUT using a Tektronix TEK-CT1 current transformer. SEB cross-section measurements were made by varying the applied drain-source voltage, since the SEB cross-section increases with increasing drain-source voltage. The SEB cross-section was

found by the usual method of dividing the total number of nondestructive current pulses per device by the beam fluence to yield units of cm²/device. The experimental test set-up is shown in Figure 1.

III. EXPERIMENTAL RESULTS

SEB cross-section measurements were obtained for the devices at device temperatures of 300 K, 333 K, 353 K, and 373 K. The cross-section versus drain-source voltage for the IR6766 and IRF150 are shown in Figures 2 and 3, respectively. In each case, the V_{DS} threshold for burnout increases with increasing temperature. Also note that in each case, for a given applied drain-source voltage, the SEB cross-section decreases with increasing temperature. Furthermore, as the drain-source bias
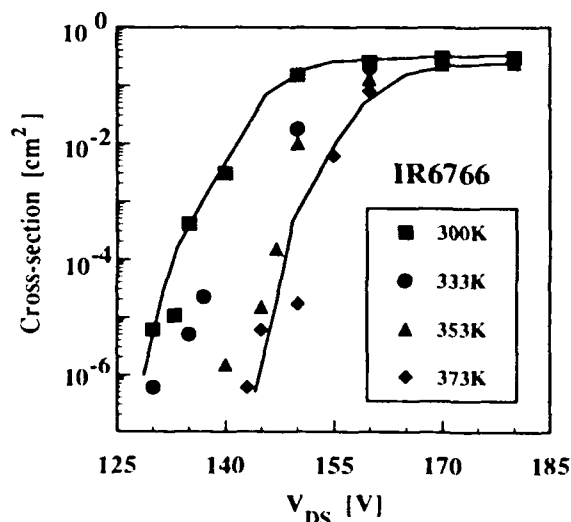

Figure 2: SEB Cross-section versus V_{DS} and temperature for the IR6766 power MOSFET (solid lines drawn to guide the eye).
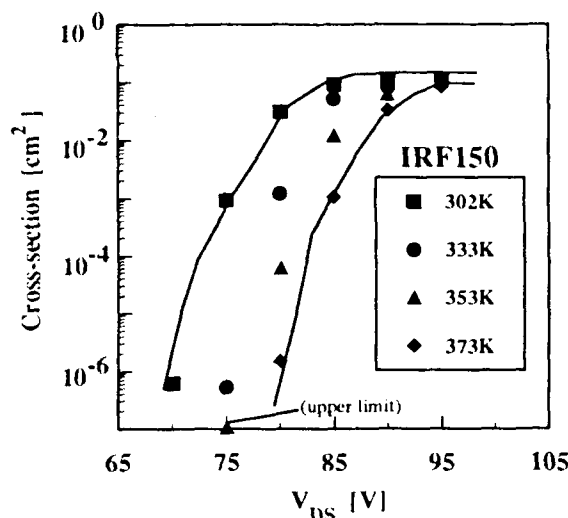
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Figure 3: SEB Cross-section versus V_{DS} and temperature for the IRF150 power MOSFET (solid lines drawn to guide the eye).

increases, the amount of change in the cross-section decreases. In other words, the burnout susceptibility decreases with increasing temperature, and the change in burnout susceptibility due to temperature decreases with increasing drain-source bias. This can be explained physically through the dependence of the impact ionization rate for electrons on temperature and electric field. The impact ionization rate for electrons decreases with increasing temperature and decreasing electric field. The data presented in Figures 2-3 are consistent with previously reported data [6]. These points and their relevance to the SEB mechanism will be explained in more detail in the next section.

IV. BURNOUT MODELING

This section will focus on the physical model of the burnout mechanism. First, the mechanism leading to burnout via the turn on of the parasitic bipolar transistor will be reviewed. Next, the manner in which temperature dependence is incorporated into the model will be discussed.

IVA. Burnout Mechanism of DMOS Structure

The cross-section of one cell in an n-channel DMOS power transistor is shown in Figure 4. A positive bias applied to the gate forms an inversion layer in the p-body region below the gate oxide, allowing electrons to flow from the source to the drain. Inherent to the DMOS structure is a parasitic npn bipolar

transistor, as shown in Figure 4. The source, body, and drain regions of the MOSFET comprise the emitter, base, and collector regions of the parasitic BJT, respectively. In normal operation of the power MOSFET, this parasitic BJT is always turned off. This is accomplished by the common source-body metallization, which shorts out the base-emitter junction of the parasitic BJT.

If lateral current flows in the body (base) below the source (emitter) region, the base-emitter junction becomes forward biased and the parasitic BJT turns on. Single-event burnout of the DMOS structure has been attributed to the turn on of this parasitic BJT [3]. If the parasitic BJT is turned ON when the MOSFET is turned OFF, second breakdown of the BJT and hence thermal meltdown (burnout), may occur. The mechanism leading to SEB will now be discussed.

Figure 4 shows the DMOS structure with a heavy ion passing through the parasitic BJT. As the heavy ion traverses the device, electron-hole pairs are generated along its track length, creating an ionized plasma filament. This plasma filament supports a short-lived current source in which holes flow up towards ground via the lateral base region, and electrons flow down towards the positively biased collector. The short-lived current source initially drives the parasitic BJT, locally turning on one cell of the DMOS structure [7].

Depending on how 'hard' the BJT is initially turned ON, the currents within the device will either regeneratively increase until burnout occurs, or the currents will die out leaving the
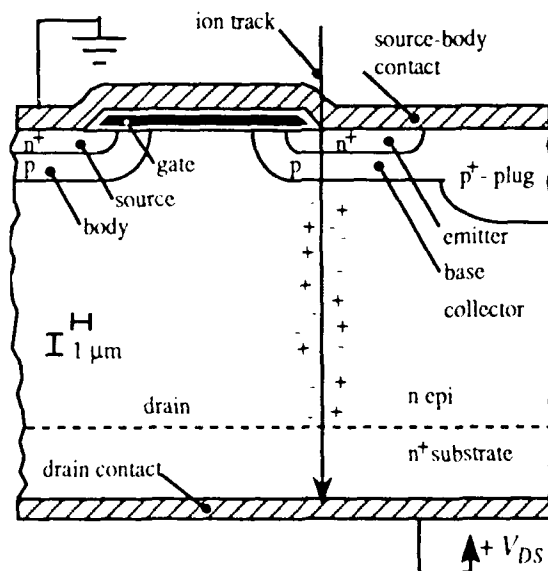

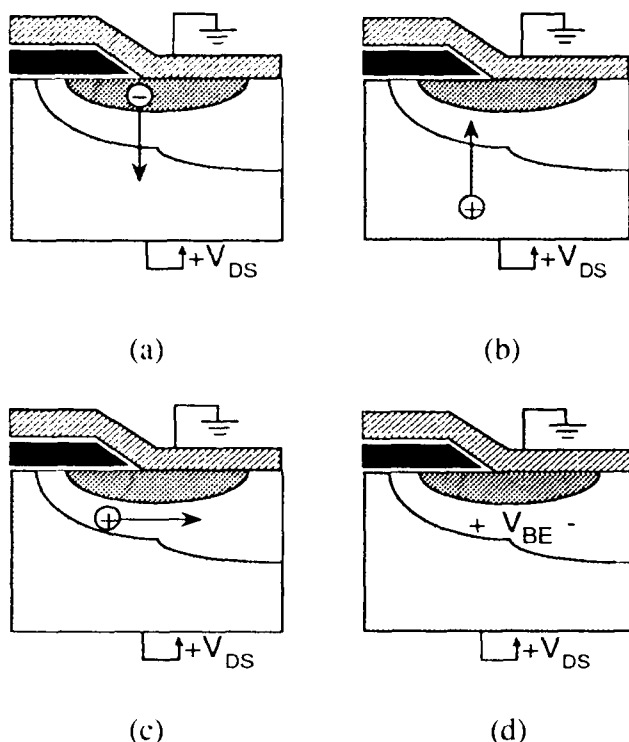Figure 4: DMOS structure showing parasitic BJT and ion track.

Figure 5: Components in feedback mechanism: (a) electron injection; (b) avalanche generated holes; (c) base current; (d) base-emitter voltage.

device unharmed. A feedback mechanism inherent to the vertical structure of the parasitic BJT will determine whether the currents will regeneratively increase or die out. The feedback mechanism consists of four basic components. These components in terms of the parasitic BJT are: (1) electron injection from the emitter across the active base into the collector; (2) avalanche-generated hole current returning from the collector into the base; (3) subsequent lateral hole current through the base to its contacts; and (4) the induced base-emitter voltage resulting from the lateral base current. The four components of the feedback mechanism are illustrated in Figure 5.

When the equations governing the feedback mechanism are solved, electron and hole current density distributions within the parasitic BJT are obtained which define the threshold for burnout [8]. The current density distributions at the threshold for burnout are called the critical condition. If the parasitic BJT is initially driven by the heavy-ion-generated current source such that currents are larger than the critical condition, then burnout occurs. If not, then the currents within the parasitic BJT die out and burnout does not occur [8].

It should be noted that in this model it seems that the position of the incident ion strike may influence how hard the parasitic BJT is driven. Incidence at the outer edge of the source region is worst case in the sense that an incident ion with the lowest LET capable of initiating burnout must strike there. At the source edge, an incident ion with a relatively low LET may induce burnout, but the same ion could not induce burnout if it were incident closer to the ground edge of the source. As one moves to positions more interior in the source region, incident ions must have higher and higher values of LET to initiate burnout. Positions more interior in the source region correspond to larger effective sensitive regions. Experimental cross-section versus LET curves show a similar trend. As the LET of the incident ion is increased, the measured cross-section increases. This same argument can be made with the cross-section versus drain-source bias curves for a constant LET that are given in this paper. As the drain-source bias is increased, an ion with the same LET can strike futher into the source region and still initiate burnout. Thus, as the drain-source bias increases, so does the sensitive region.

The temperature dependence of the burnout mechanism can be readily introduced into this feedback mechanism and will now be outlined.

IVB. Temperature Dependence

In the foregoing discussion, it should be emphasized that the primary component of the burnout mechanism is the base current density flowing in the parasitic BJT. In order for the parasitic BJT to turn on and remain turned on, it must have a source of base current. Unlike 'normal' BJT operation, the base current is not supplied from a device terminal; rather, the base current is supplied through avalanche multiplication in the base-collector space charge region (SCR). It will later be shown that the hole current generated in the base-collector SCR is a function of the doping density and thickness of the collector region, the applied drain-source bias, and the local injected electron density [8]. In the following discussion on the temperature dependence of the burnout mechanism, the focus will be on the base current generated through avalanche multiplication. In other words, the injected electron density will be held 'constant' as a function of temperature, and the change of avalanche generated holes will be
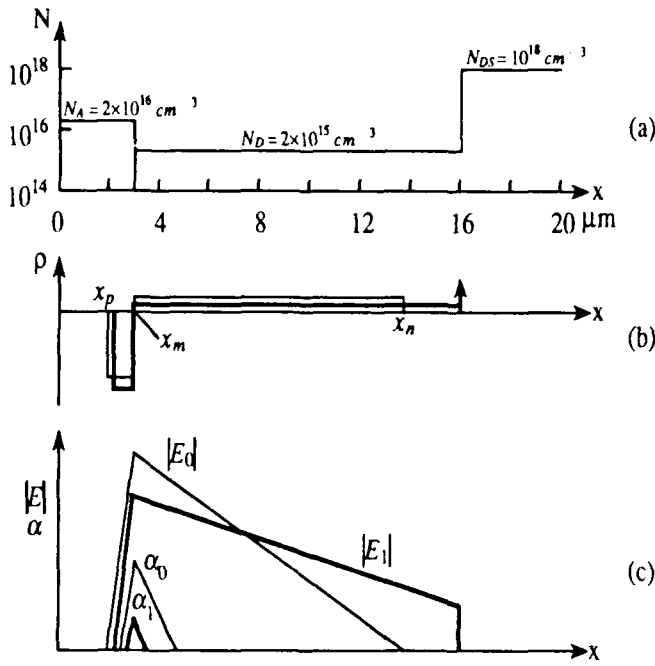
Figure 6: (a) idealized doping densities in base-collector space charge regions; (b) charge densities for zero and nonzero currents; and (c) electric field and impact ionization rate profiles for zero and nonzero currents.

monitored as a function of temperature. This is equivalent to accounting for the 2-3mV/°C decrease of base-emitter voltage in the parasitic BJT.

As mentioned previously, the avalanche generated hole current is a function of the doping density and thickness of the collector region, applied drain-source voltage, and the local injected electron density within the base-collector space charge region. The complete details for calculating the avalanche generated hole current appear in [8]. Only the major points will be described here.

The one dimensional Poisson equation is solved across the base collector depletion region taking into account the space charge associated with the mobile carriers. When the space charge of the mobile carriers is considered, the electric field across the base collector space charge region will be somewhat altered, depending on the density of mobile charge compared to the density of background impurity charge. A qualitative illustration of how the electric field is changed is shown in Figure 6 [8]. An idealized impurity profile through the base, collector, and substrate of the parasitic BJT in a typical power MOSFET is shown in Figure 6a. The two cases of zero and non-zero current are depicted in Figures 6b and 6c. The light lines correspond to

the zero current case, and the heavy lines correspond to the non zero current case. The electric field and ionization rate plots are further labelled with the subscripts 0 and 1 to distinguish between zero and non-zero currents respectively. The total charge density for the non-zero current case, shown in Figure 6b, has changed to reflect the electrons in transit across the junction. The total charge density to the left of the metallurgical junction, x_m, is more negative (the electrons add to the total charge), and the total charge density to the right of the metallurgical junction is less positive than for the zero current case (the electrons subtract from the total charge).

The change in the total charge density is also reflected in the electric field distribution, shown in Figure 6c. Since the total charge density is more negative to the left of x_m for non-zero current, the electric field in this region will have a steeper slope than for the zero current case. This effectively lowers the peak electric field at x_m and moves x_p to the right. Similarly, since the total charge density is less positive to the right of x_m for non-zero current, the electric field in this region will have a lower gradient than for the zero current case. Since the reverse bias for each case is the same, the area under each electric field plot must be equal. This equal area constraint and the lower slope to the right of x_m, push the right edge of the electric field, x_n, deeper into the collector region. In the example shown in Figure 6c, x_n, has reached the epi-substrate boundary at which point the electric field can penetrate no further. The electric field will assume a non-zero value at the epi-substrate boundary to satisfy the equal area constraint imposed by the boundary conditions of the Poisson equation. Therefore, two important phenomena occur in the reverse biased base collector junction when non-zero current flows: (1) the peak electric field at the metallurgical junction decreases, and (2) the electric field assumes a non-zero value at the epi-substrate interface. These two consequences significantly affect the avalanche multiplication, as will be shown later.

The impact ionization rate, α, throughout the depletion region for zero and non-zero current is also shown in Figure 6c. The impact ionization rate, α, is exponentially related to the local electric field [8]. This is why the value of α decreases significantly when the peak electric field drops with increasing current. The avalanche multiplication rate, M, significantly decreases with increasing current as well. The functional relationships between carrier densities, electric field, ionization rate, applied
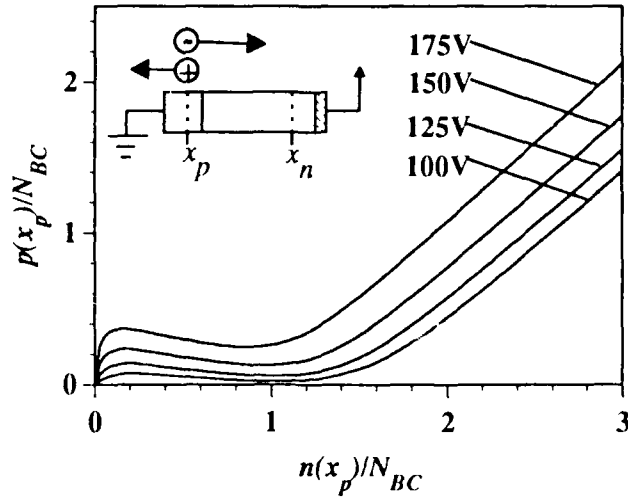
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Figure 7: Avalanche curves at 300K for 100 V, 125 V, 150 V, and 175 V for device with nominal breakdown voltage of 190 V.

voltage, and the physical geometry of the parasitic BJT must be simultaneously solved to determine the avalanche multiplication rate, i.e., the density of avalanche generated holes returning to the neutral base for a given injected electron density.

Recall that the desired result is the hole concentration at x_p, $p(x_p)$, as a function of electron concentration at x_p, $n(x_p)$, or:

$$M = \frac{p(x_p)}{n(x_p)}. \qquad (1)$$

There are six arrays of typically 300 points used in the calculation (the depletion region is discretized into 300 points). These arrays are: (1) space charge, $\rho(x)$; (2) electric field, $E(x)$; (3) potential, $V(x)$; (4) ionization rate, $\alpha(x)$; (5) electron concentration, $n(x)$; and (6) hole concentration, $p(x)$. Given the impurity profile, the applied drain to source voltage, V_{DS}, and the electron concentration at x_p, the profiles of $\rho(x)$, $E(x)$, $V(x)$, $n(x)$, $p(x)$, and $\alpha(x)$ are calculated for self-consistency [8].

The equations, sample calculations of electric field, ionization rate, potential, carrier densities, and other details of this calculation appear in [8]. The end result is plotted in Figure 7, which shows the calculated avalanche curves for a device with a nominal BV_{DS} of 190 V. There are three distinct regions present in each avalanche curve shown in Figure 7. The first region is the distinct hump appearing for values of $n(x_p)/N_D < 1$. This corresponds to an initial decrease in the avalanching rate with increasing current. The second region is the valley region or local minimum appearing for values of $n(x_p)/N_D = 1$. This corresponds

to a near zero avalanching rate at a current level where the injected electron density and collector doping density are comparable. The third region of the avalanche curve appears for values of $n(x_p)/N_D > 1$, where the hole concentration increases at approximately the same rate as the electron concentration.

In terms of the feedback mechanism for SEB, the appropriate value for M can be obtained from a curve similar to Figure 7. Note that it is necessary to calculate a separate avalanche curve for each device structure and each applied drain-source bias when solving the equations governing the feedback mechanism.

The temperature dependence is included in the aforementioned calculation via the impact ionization rate. The impact ionization rate (number of electron-hole pairs generated per unit path length) decreases with increasing temperature [9]. This is attributed to the shorter mean free path of the carriers. Since the impact ionization rate is used explicitly in the solution to the Poisson equation, the avalanche-generated hole current density decreases with increasing temperature for the same injected electron current density and applied drain-source bias. A measure of the reduction in hole current density is shown in Figure 8. The ratio of the hole density retuning to the base at 400 K, p_{400}, and the hole density at 300 K, p_{300}, is plotted as a function of the electron density, n, injected into the base-collector space charge region of the parasitic BJT. The electron density has been normalized to the doping density in the collector, N_D. Note that the hole density at 400 K ranges from 30% to 90% of the hole
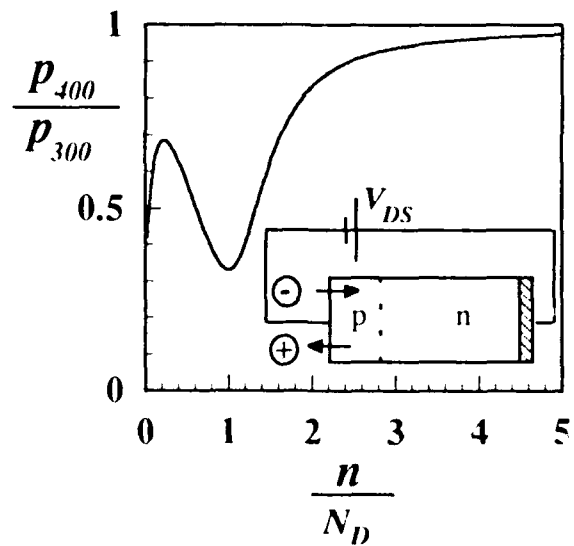

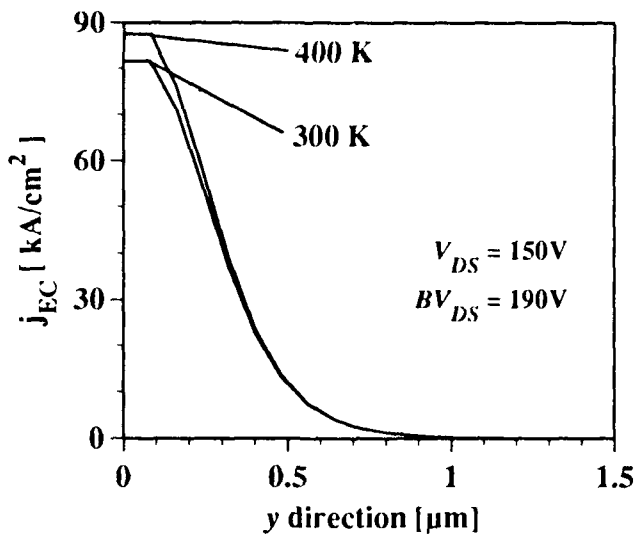Figure 8: Ratio of avalanche curves at 400 K and 300 K.

Figure 9: Critical electron current density distribution in the collector at the threshold for burnout with drain-source bias of 150 V at 300 K and 400 K.

Figure 10: Calculated SEB threshold as a function of temperature and drain-source bias.

density at 300 K over much of the operating region. This reduction of the source of base current at higher temperatures is equivalent to an increase of the burnout threshold of the device (ie, in order to achieve the same level of base current, the electron current density in the collector must increase). The calculated temperature dependence of the burnout threshold will be presented in the next section.

V. CALCULATED TEMPERATURE DEPENDENCE

The relationships governing the feedback mechanism can be solved to yield a collector current density distribution at the threshold for burnout, j_{EC}, for a given DMOS device structure [8]. Figure 9 shows the threshold j_{EC} plotted against position in the parasitic BJT for temperatures of 300K and 400K. These calculations indicate that the peak j_{EC} increases from 81.5 kA/cm² to 87.5 kA/cm² when the temperature increases from 300K to 400K. When the critical collector current density is integrated around one cell of the DMOS structure, a critical collector current for burnout is obtained. The critical collector current for burnout, calculated as a function of drain-source voltage and for ambient temperatures of 300K and 400K, is plotted in Figure 10. The device structure used in these calculations has a nominal break-down voltage of 190V. The device structure used in the calculations is similar to the experimental samples only in the sense that they each have similar values of BV_{DS}. No attempt was made to
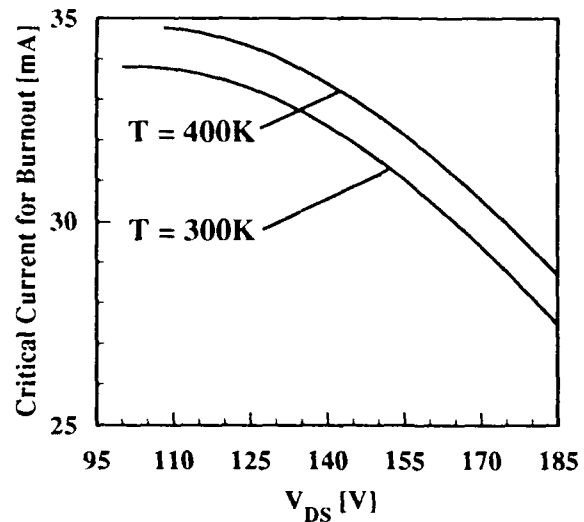
determine actual dimensions and doping distributions of the experimental samples. For the calculations, the average doping densities in the source, p-body, p⁺-plug, and drain region are 10^{21} cm⁻³, 2×10^{17} cm⁻³, 2×10^{19} cm⁻³, and 2×10^{15} cm⁻³, respectively. The thickness of the drain region is 13 μm. As shown in Figure 10, the SEB threshold increases with increasing temperature and decreasing voltage. Note that an increase of the critical current increases the SEB threshold. Furthermore, the increase of the SEB threshold is more pronounced at the lower drain-source biases. Once again, this is a result of the temperature and electric field dependence of the impact ionization rate for electrons. Therefore, the SEB threshold has increased by approximately 2.9% for a 100 degree temperature increase at the higher drain-source biases, and the SEB threshold has increased by approximately 4.4 % at the lower drain-source biases. These results are consistent with the experimental trends previously discussed.

VI. SUMMARY AND CONCLUSIONS

In this paper, the temperature dependence of SEB in power DMOS devices was discussed. Experimental data for the IR6766 and IRF150 power MOSFETs were presented. The data indicate a definite temperature dependence of the burnout cross-section and in the threshold value of drain-source bias required for burnout. Temperature dependence was included in an existing SEB model through the impact ionization rate, and the

calculated results agreed with the experimental trends.

From the results presented in this paper, one can conclude that power DMOS devices are more resistant to SEB when operated at an elevated temperature. This is an important issue for systems that may be operated outside of the 300 K regime in the space radiation environment.

VII. ACKNOWLEDGEMENTS

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III. Single-Event Burnout of Power Bipolar Transistors

III.A Introduction

Work was conducted in this area in cooperation with Jeff Titus at NWSC-Crane. Jeff exposed a variety of power BJTs to heavy ions at Brookhaven National Labs and determined their threshold LETs for burnout as a function of bias conditions. The experiment included both single transistors and Darlington pairs. This was the first reported observance of single event burnout in power BJTs.

The experimental results were analyzed using the power-MOSFET single-event burnout model described in Section II, and the results were presented in a paper at the 1991 IEEE Nuclear and Space Radiation Effects Conference. The paper is summarized here and the text is included in Section III.B.

Section III.B: J.L. Titus, G.H. Johnson, R.D. Schrimpf, and K.F. Galloway, "Single Event Burnout of Power Bipolar Junction Transistors," *IEEE Trans. Nucl. Sci.*, vol. NS-38, pp. 1315-1322, 1991.

This paper presents experimental evidence that power bipolar junction transistors are susceptible to catastrophic failure in a cosmic ray environment. Several types of commercially available power transistors were characterized using the tandem van de Graaff accelerator at Brookhaven National Laboratory. Most device types that were exposed to a mono-energetic ion with an LET greater than 27 MeV-cm^2/mg exhibited burnout at collector-emitter voltages less than their rated breakdown voltage. Failure analysis performed on burned-out devices indicates that the failure mechanism is similar to thermal runaway induced by second breakdown. A semi-analytical model was developed to explain this failure mechanism. The model suggests a strong correlation between single-event burnout susceptibility and key layout and processing parameters. The experimental results dictate that system designers should seriously consider the impact of single-event burnout of power bipolar transistors in space applications.

This paper won the Outstanding Conference Paper award at the 1991 IEEE Nuclear and Space Radiation Effects Conference.

III.B Single Event Burnout of Power Bipolar Junction Transistors

SINGLE-EVENT BURNOUT OF POWER BIPOLAR JUNCTION TRANSISTORS[†]

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ABSTRACT

Experimental evidence of single-event burnout of power bipolar junction transistors (BJTs) is reported for the first time. Several commercial power BJTs were characterized in a simulated cosmic ray environment using mono-energetic ions at the tandem Van de Graaff accelerator facility at Brookhaven National Laboratory. Most of the device types exposed to this simulated environment exhibited burnout behavior. The experimental technique, data, and results are presented, while a qualitative model is used to help explain those results and trends observed in this experiment.

I. INTRODUCTION

As system designers began to incorporate power metal oxide semiconductor field effect transistors (MOSFETs) into spaceborne applications, single-event burnout (SEB) was identified as a possible catastrophic failure mode. Power MOSFET burnout has been attributed to the parasitic bipolar junction transistor (BJT) inherent to the double-diffused MOS (DMOS) structure [1]. In previous characterization of burnout in the power DMOS structure it was believed that in order for burnout to occur, the drain-source voltage of the MOSFET must exceed the open circuit collector-emitter breakdown voltage (BV_{CEO}) of the parasitic BJT. This paper reports that the power BJT is susceptible to burnout even when biased below its measured BV_{CEO}.

Several commercial power BJTs were exposed to mono-energetic ions in the tandem Van de Graaff accelerator facility at Brookhaven National Laboratory (BNL). The majority of the power BJTs were single devices, although several integrated Darlington pairs were included. All but two of the transistor types exhibited single-event burnout. The experimental technique, data, and results are presented in Section II. A model for the burnout mechanism in

power BJTs, similar to that used for power MOSFET burnout [2], is used to help explain the trends in the experimental data. This model is discussed in Section III. The experimental trends in the data are explained within the context of the model in Section IV. Finally, conclusions are made concerning the susceptibility of power BJTs; and design methodologies are suggested to assist in fabricating more robust power BJTs in Section V.

II. POWER BJT BURNOUT EXPERIMENT

This section of the paper discusses the details of the power BJT single-event burnout experiment. The device types used in the experiment are presented first. Second, the test setup is described. Next, specifics of the experimental testing technique are mentioned. And finally, a summary of the results of the experiment is given.

A. Experimental Test Samples

Test samples were acquired that had various structural parameters and layout geometries. There were a total of nine device types, of which all but one were commercially available. The one device type that was not commercially available was an experimental transistor which incorporated numerous process and design techniques that were believed to decrease its susceptibility to single-event burnout. The experimental device will be referred to as 2NXXXX. All device types were obtained in sufficient quantities to perform a thorough characterization except for the 2N3055 and the 2N4033. These two device types were obtained only in a very small quantity and a complete characterization was not performed. A detailed description of the physical parameters for each device type is presented in Table 1.

The data shown in Table 1 consist of the device type, structural information obtained through angle-lapping techniques, and their rated breakdown voltages. Actual collector-emitter open circuit breakdown voltage (BV_{CEO}) and collector-base open circuit breakdown voltage (BV_{CBO}) measurements were made on most test samples. Three of the

Device Type	Emitter Junction Depth (µm)	Base Junction Depth (µm)	Epitaxial Layer Thickness (µm)	Rated V$_{CEO}$ (V)
2N5629	6.35	28.96	46.74	100
2N6056	6.60	22.86	30.23	80
2N6059	18.03	21.08	27.94	100
2N6284	6.10	20.07	32.77	100
MJ15003	10.41	34.29	50.29	140
2N3902	12.45	29.21	108.20	400
2N3055	60.96	86.61	100.80	60
2NXXXX	3.05	5.33	24.89	60
2N4033				80

Table 1: Characteristics of selected test devices.

Figure 1: Experimental test circuit.

nine device types tested were Darlington pairs and are identified as 2N6056, 2N6059, and 2N6284. All test samples were physically delidded prior to heavy ion bombardment.

B. Experimental Test Setup

The experimental test technique employed was similar to other non destructive test techniques that were previously used to characterize power MOSFETs [3, 4]. The test circuitry is shown schematically in Figure 1. The base and emitter terminals were shorted to a common ground, while the collector terminal was biased to a specific voltage. The collector-emitter bias remained constant while the device was exposed to the ion beam and was changed only at the end of each test run in which burnout did not occur.

Single event burnout cross sections (ie., effective critical device area plotted against LET) were not obtained due to the variety of current pulse heights observed. Separating the actual burnout pulse from the other current pulses was not possible with the test equipment and test fixture that was employed. Therefore, burnout was verified by removing any current limiting resistances in the collector lead and by increasing the value of the stiffening capacitance, $C\alpha$, connected across the device under test (DUT). Both techniques, removal of external resistance and addition of a large stiffening capacitance, were needed to actually induce BJT burnout. These changes in the test circuit made this a destructive test (ie., devices exhibiting burnout were damaged and became nonfunctional).

Any resistance between the collector lead and stiffening capacitor seemed to prevent burnout, although current pulses were observed. Also, the stiffening capacitance had to exceed a certain value, or burnout was circumvented. A stiffening capacitance of 5 µF or greater was sufficient in all cases. Burnout was monitored using a Tektronix CT-2 current probe between the stiffening capacitor and ground. The output of the current probe was connected directly to a storage oscilloscope, allowing the pulses to be captured. A reconstruction of a
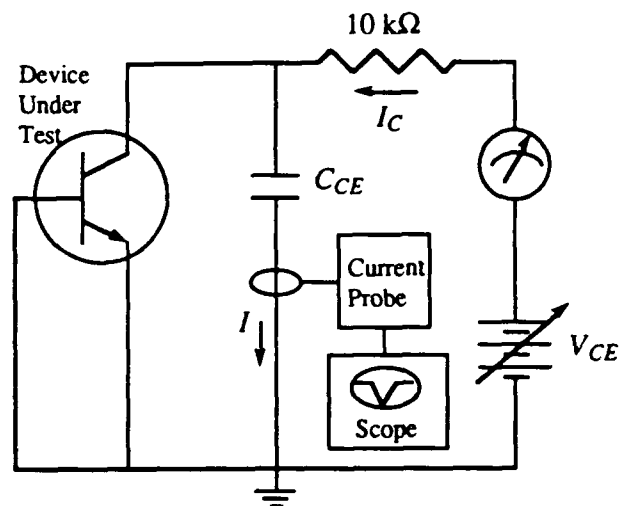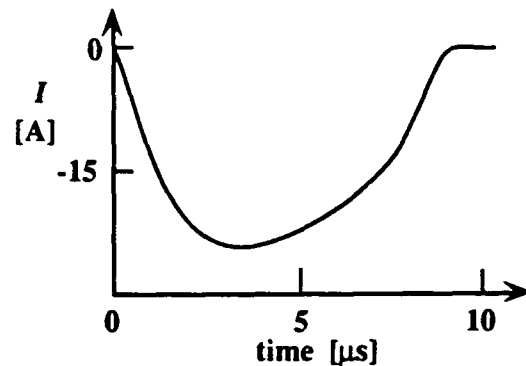

Figure 2: Reconstructed burnout pulse measured from current probe.

typical burnout pulse measured from the current probe is shown in Figure 2. The collector current was also monitored directly with an ammeter connected between the stiffening capacitors and the power supply so that, if the burnout pulse was not captured, a sudden and dramatic increase in collector current would indicate that burnout had indeed occurred.

C. Experimental Test Techniques

Nine different NPN bipolar device types were characterized using the test setup just described in a simulated cosmic ray environment using heavy ions obtained from the tandem Van de Graaff accelerator facility at Brookhaven National Laboratory. Specific mono-energetic ion species were chosen to span a linear energy transfer (LET) range from 27 to 80 MeV-cm^2/mg and penetration depths or ranges in silicon from 42 to 25 µm, respectively. Ion penetration depth is thought to be critical to the test measurement and the burnout sensitivity of the power BJT. Penetration depth has been shown to be relevant in LET threshold measurements of power MOSFETs [5]. These same concepts apply to power

Symbol	Element	Energy [MeV]	LET $\left[\dfrac{MeV \cdot cm^2}{mg}\right]$	Range [μm]
^{197}Au	Gold	350	80	25
^{127}I	Iodine	320	60	31
^{79}Br	Bromine	285	37	37
^{58}Ni	Nickel	265	27	42

Table 2: Selected Mono-Energetic Ion Characteristics.

BJTs as well. The characteristics of each selected ion are shown in Table 2.

The normal test sequence used during SEB characterization went as follows: (1) the device was exposed to a fixed particle fluence, during which the collector current was monitored; (2) if burnout was not observed, the collector voltage was increased by typically 2 to $10V$, upon which step (1) was repeated; and (3) the test sequence was terminated if burnout was observed or a predetermined collector voltage was reached. However, all test sequences were terminated if the collector voltage reached 334 volts, due to voltage constraints of the power source and the voltage ratings of the capacitors used in the test circuit. In some later experiments, the test voltage was limited to 400 V after some minor modification to the test circuitry was made. All experiments were performed under D.C. bias with the collector voltage of the device initially set lower than the expected voltage needed to induce device burnout - the SEB threshold voltage of the device for a given LET. The DUT was exposed to the selected ion species until a fluence of 1.0×10^6 ions/cm² was obtained. The test sequence was only interrupted if burnout was observed.

D. Summary of Experimental Results

More than 400 individual runs were recorded at BNL. During these runs, over 40 test devices were exposed to one or more ion species. A summary of the test results is provided in Table 3. This table identifies the following key parameters: the device type and serial number; the LET of the ion species; the breakdown voltages of the device, BV_{CEO} and BV_{CBO}; the highest collector voltage at which burnout was not observed; and the collector voltage at which burnout was observed. The four devices which exhibited repeated burnout behavior (2N5629, 2N6056, 2N6059, and MJ15003) are shown in Figure 3. The collector-emitter voltage normalized to the measured BV_{CEO} is plotted against the LET of the incident ion. Each bar represents one single device. The dark shaded region represents the difference between the normalized voltage that the device exhibited burnout and the highest normalized voltage that the device did not burnout. Notice that the Darlington pairs, 2N6056 and 2N6059, are more susceptible to burnout than the single devices, 2N5629 and

Device	LET $\left[\dfrac{MeV \cdot cm^2}{mg}\right]$	Measured BV_{CEO} [V]	Measured BV_{CBO} [V]	Pass V_{CE} [V]	Fail V_{CE} [V]
2N5629-10	27	225	520	190	195
2N5629-07	37	270	550	195	200
2N5629-11	60	180	520	145	150
2N5629-12	80	180	540	170	180
2N6056-08	27	220	220	52	54
2N6056-07	37	150	150	48	50
2N6056-09	60	200	200	46	48
2N6056-09	80	200	200	50	55
2N6056-10	80	210	210	45	50
2N6059-10	27	200	200	50	51
2N6059-09	37	234	234	52	54
2N6059-11	60	170	170	45	48
2N6059-13	80	245	245	45	50
2N6284-12	27	130	130	130	---
2N6284-07	27	110	110	110	---
2N6284-07	37	110	110	110	---
2N6284-12	60	130	130	90	100
2N6284-08	60	110	110	110	---
2N6284-10	80	120	120	110	---
2N6284-08	80	110	110	110	---
MJ15003-09	27	270	480	220	240
MJ15005-08	27	250	320	----	190
MJ15003-06	37	230	430	195	200
MJ15003-07	37	270	500	215	218
MJ15003-10	60	280	430	200	210
MJ15003-03	60	270	490	200	205
MJ15003-11	80	230	430	200	210
2N3902-05	27	830	990	334	---
2N3902-09	27	650	700	334	---
2N3902-05	37	830	990	334	---
2N3902-05	60	830	990	334	---
2N3902-05	80	830	990	400	---
2NXXXX-102	27	60	150	130	---
2NXXXX-102	37	60	150	130	---
2NXXXX-102	60	60	150	130	---
2NXXXX-102	80	60	150	130	---

Table 3: Summary of SEB test results.

MJ15003. The collector-emitter biases that resulted in burnout behavior are consistent with high dose-rate burnout in power BJTs [6].

III. POWER BJT BURNOUT MECHANISM

This section will address the mechanism that leads to burnout of the power BJT. First, the structure of a typical power BJT is discussed. Second, the burnout mechanism is described; and the key structural parameters that lead to
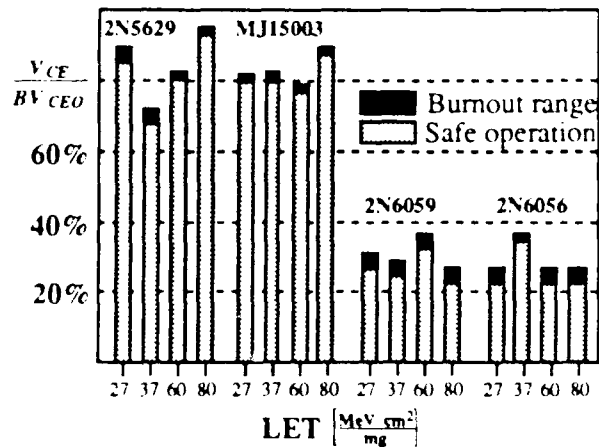
Figure 3. Burnout test results.

Figure 4 Power BJT Device Structure.

burnout are pointed out. And finally, a calculation of the burnout threshold for a realistic device structure is presented.

A. The Power BJT Device Structure

When operating as a switch, a power BJT must be capable of blocking a large voltage when it is turned off and conducting a large current when it is turned on. The high voltage and high current capabilities of the power BJT result from the device structure shown in Figure 4. The power BJT is similar in appearance to an integrated BJT with the exception that the collector is contacted on the back surface of the chip. This backside contact allows the designer to use a thick epitaxial layer. The thickness and doping density of this epitaxial layer dictate the voltage that the BJT can block when it is turned off. A thicker and more lightly doped epitaxial layer yields a higher blocking voltage than a thinner or more heavily doped layer [7]. For a BJT, a large emitter area is necessary in order to achieve high conduction currents for a given current density [8]. In a power BJT, the large emitter area is obtained by using several emitter stripes. This segmentation of the emitter reduces current crowding effects that reduce the collector current for a given base-emitter bias [9]. Although the device shown in Figure 4 has two emitter stripes, an actual device may have many more. In the power BJT, each emitter stripe is contacted by one common emitter metallization, and the base region is contacted between each emitter stripe by one common base metallization. For clarity, the base and emitter contact metallizations have not been shown in Figure 4.

B. The Power BJT Burnout Mechanism

The vertical structure of the power BJT is very similar to that of the parasitic BJT inherent to the power DMOS device. The parasitic BJT has been attributed to burnout in the DMOS structure [2], and the burnout mechanism in power BJTs is similar to that in power MOSFETs. A schematic cross
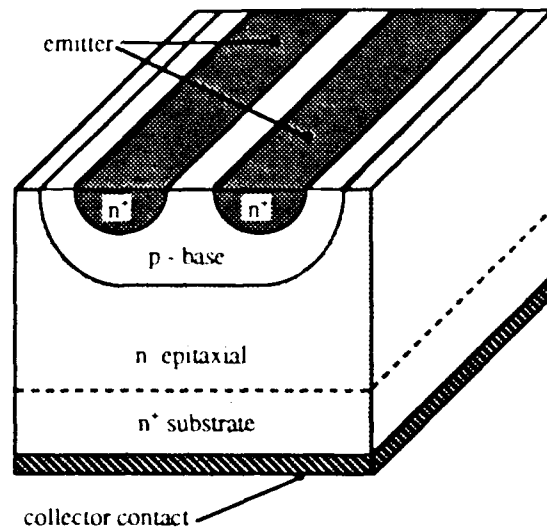
section of the power BJT structure, including an incident ion track, is shown in Figure 5.

As the heavy ion traverses the device, electron-hole pairs are generated along its track length creating an ionized plasma filament. This plasma filament supports a short-lived current source in which holes flow towards ground via the lateral base region, and electrons flow down towards the collector. The hole current locally forward biases the base-emitter junction, turning on the BJT [10].

Now, depending on how hard the BJT is initially turned on, currents within the device will either: regeneratively increase until the simultaneous high current and high voltage in the device trigger second breakdown and consequently
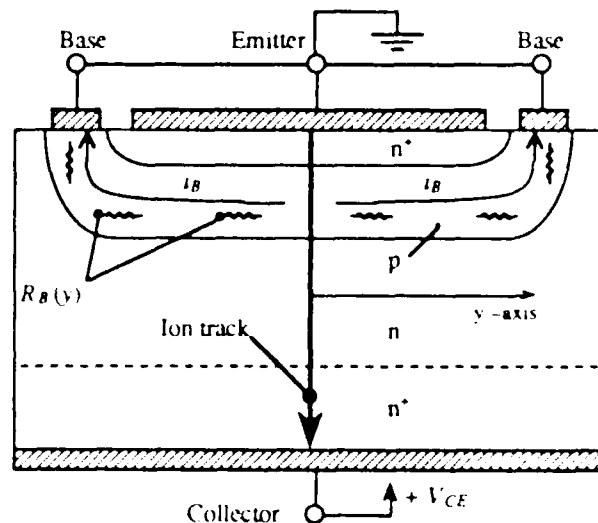

Figure 5 Cross section of power BJT with heavy ion track

thermal meltdown, or the currents will die out to zero leaving the device unharmed. A feedback mechanism inherent to the device structure dictates whether the currents will regeneratively increase or decrease.

The feedback mechanism relates: (1) electron injection from the emitter across the active base into the collector; (2) avalanche-generated hole current returning from the collector into the base; (3) subsequent lateral hole current through the base to its contacts; and (4) the induced base-emitter voltage resulting from this lateral base current. A similar feedback mechanism was proposed for the power DMOS structure [11]. The equations governing the feedback mechanism will now be discussed.

The coordinate system for this model is shown in Figure 5. The origin is defined at the point of the ion strike. Now, assuming a potential, $V_{BE}(y)$, exists that is large enough to locally turn on one finger of the power BJT, the electron current density injected by the emitter, $j_{EC}(y)$, can be expressed to first order by: [8]

$$j_{EC}(y) = \frac{q D_n n_i^2}{N_{AB} w_B} \exp\left[\frac{V_{BE}(y)}{kT/q}\right],$$ (1)

where q, D_n, n_i, N_{AB}, w_B, k, and T correspond to the electronic charge, electron diffusivity, intrinsic doping density, doping density in the base region, active base width , Boltzman constant, and absolute temperature, respectively.

Since the base-collector junction has a large reverse bias applied across it, the electric field will be large throughout much of the collector region. Therefore, for each electron injected across the base into the collector, there will be avalanche-generated holes returning to the base region. The avalanche-generated hole current density, $j_{HC}(y)$, is given by: [11]

$$j_{HC}(y) = M q v_{sat}\left\{\frac{D_n n_i^2}{v_{sat} N_{AB} w_B} \exp\left[\frac{V_{BE}(y)}{kT/q}\right]\right\},$$ (2)

where v_{sat} is the saturation velocity for electrons. The multiplication factor, M, in equation (2) is defined as the ratio of hole density to the electron density at the base side of the base-collector space charge region (SCR). M is a function of the electric field, ionization rate, and the injected electron density, and is obtained numerically [11]. The term within the curly brackets in equation (2) is the electron density at the base edge of the base-collector SCR, including the Kirk effect [12].

Due to the forward bias, $V_{BE}(y)$, there also exists a back-injected hole current density, $j_{HE}(y)$. This current density is expressed to first order by [8]:

$$j_{HE}(y) = \frac{q D_p n_i^2}{N_{DE} L_p} \exp\left[\frac{V_{BE}(y)}{kT/q}\right],$$ (3)

where D_p, N_{DE}, and L_p correspond to the diffusivity of holes, doping density in the emitter, and the diffusion length of holes, respectively.

There is one remaining current in the feedback mechanism to be described. This is the incremental hole current density which flows laterally through the neutral base region to the ground contact and develops the Ohmic drop necessary to keep the base-emitter junction forward biased. The value of this incremental current density, $j_{HB}(y)$, at any point y is simply the difference between the avalanche-generated hole current density and the back-injected hole current density, which is:

$$j_{HB}(y) = j_{HC}(y) - j_{HE}(y).$$ (4)

Next, a second order differential equation can be formulated that relates the Ohmic drop to the current density in the neutral base region [11]. First, the incremental lateral base current is just the local incremental base current density:

$$\frac{d i_B(y)}{d y} = j_{HB}(y).$$ (5)

Second, the incremental voltage drop is given by:

$$\frac{d V_{BE}(y)}{d y} = -R_B(y) i_B(y).$$ (6)

Equations (5) and (6) can be combined to give:

$$\frac{d^2 V_{BE}(y)}{d y^2} = -R_B(y) j_{HB}(y).$$ (7)

Equations (2-4) and (7) can be solved to obtain a critical condition necessary to initiate burnout [11]. This calculation will be illustrated in the next section for a specific device structure.

C. Power BJT Burnout Calculation

A device structure very similar to the 2N5629 will be used for the calculations in this section. First, the critical condition for burnout will be calculated for a given collector bias. Then, the effects of collector bias and emitter stripe width, w_E, on the critical condition will be examined. The following parameters will remain constant throughout the calculations: emitter doping density = 2×10^{20} cm^{-3}, base doping density = 2×10^{16} cm^{-3}, collector doping density = 5.5×10^{14} cm^{-3}, emitter diffusion depth = 6.4 μm, base diffusion depth = 29 μm, and epitaxial layer thickness = 42 μm. For a given emitter stripe width, w_E, the worst case ion strike is right in the center of the stripe; therefore, the origin of the y-axis will be at the center of the emitter stripe in each case. The maximum value of y, y_P, is defined to be at the lateral edge of the emitter stripe as shown in Figure 6.

The solution to equations (2)-(4) and (7) is shown in Figures 7-9. The collector bias for this case is 250V, and the emitter stripe width is 300 μm. Shown in Figure 7 is the hole current density profile in the base region. The base current per emitter finger length is shown in Figure 8, and the base-
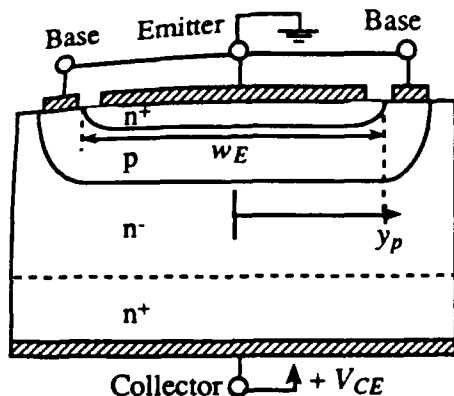
Figure 6: Power BJT structure for calculation.

Figure 8: Critical base current density for burnout.

emitter voltage is shown in Figure 9. These curves represent the critical condition for burnout because any heavy-ion generated perturbation in the system larger than that given in Figures 7-9 will result in regeneratively increasing currents within the device and thus burnout occurs [11]. If the heavy-ion generated perturbation is less than that given in Figures 7-9, the currents will decay to zero; and burnout does not occur.

Any of the curves in Figures 7-9 can be used as a figure of merit of the burnout susceptibility of the device. For the next two calculations, the saturating value of base current per length of emitter stripe in Figure 8 will be used to assess the burnout susceptibility.

The effect of collector bias on the burnout susceptibility is shown in Figure 10. For this calculation, the collector bias was varied from 250V to 450V, and the emitter stripe width remained constant at 300 μm. Note that the amount of base current necessary to initiate burnout decreases as the collector bias increases (ie., the burnout susceptibility increases with increasing collector bias).

The effect of the emitter stripe width, w_E, on the burnout susceptibility is shown in Figure 11. For this calculation, w_E
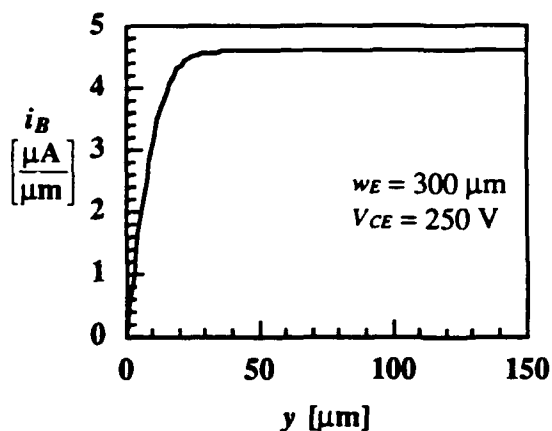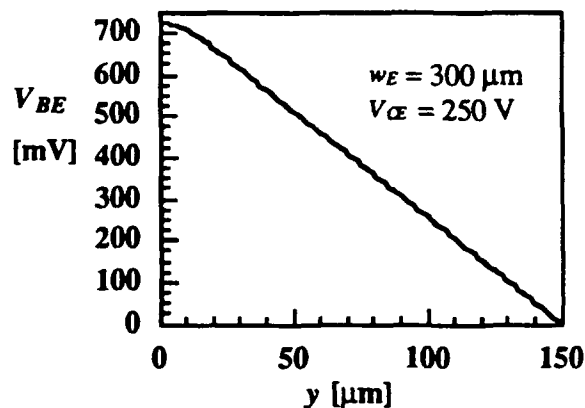

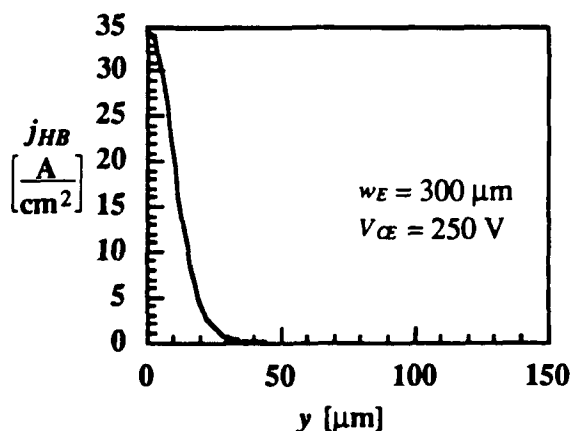Figure 9: Critical base-emitter voltage for burnout.

Figure 7: Critical incremental base current density for burnout.
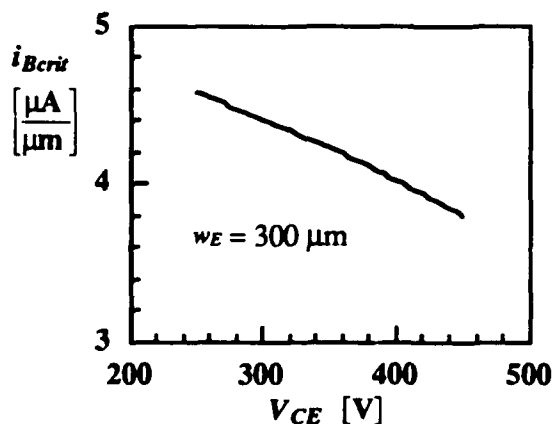

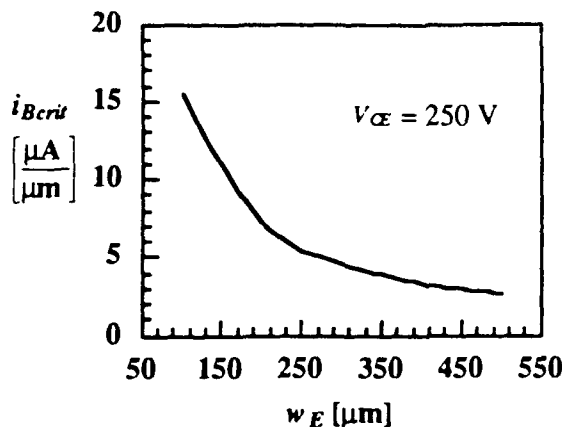Figure 10: Collector bias dependence on burnout susceptibility.

Figure 11: Emitter stripe width dependence on burnout susceptibility.

was varied from 100 μm to 500μm while the collector bias remained constant at 250V. Note that the burnout susceptibility increases as the emitter stripe width is increased.

IV. RESULTS AND DISCUSSION

The test results revealed that commercially available power BJTs are susceptible to single event burnout. Six of the nine device types tested (2N5629, 2N6056, 2N6059, MJ15003, 2N6284, and 2N4033) experienced burnout. The collector-emitter bias voltage was below the measured BV_{CEO} in all cases, and in some cases the collector-emitter bias voltage was below the rated BV_{CEO}. This observation is important; because, system designers may not derate power BJTs enough to prevent single event burnout.

The model for the burnout mechanism predicts that the burnout threshold is weakly dependent on the applied V_{CE}, according to Figure 10. If V_{CB} is increased ($V_{CB} = V_{CE}$ in the experimental set up), the avalanche-generated hole current is increased which in turn increases the hole current flowing laterally through the base region. The data shown in Figure 3 does not show this V_{CE} dependence, however. This discrepancy in the model and the experimental data can best be explained by the penetration depth in silicon of the incident ion. Recall that as the LET of the incident ion is increased, the penetration depth in silicon decreases. The current source associated with the plasma filament along the ion track begins to spread out conically towards the end of the ion track. This results in an increased area that the current flows through and thus reduces the current density in the high field region of the base-collector SCR [5]. Therefore, the BJT is not initially driven as hard as it would for a longer penetration depth.

Recall that the Darlington pairs that exhibited burnout did so at collector biases much lower than the single BJTs that exhibited burnout. The Darlington pair is more susceptible to burnout because of its high gain. The input transistor is most vulnerable because its emitter current is fed into the base of the output transistor. Therefore, a much smaller initial base current density is necessary to drive the pair into burnout.

Some of the commercially available power BJTs did not

exhibit burnout. The data from these devices can be best explained by examining their measured electrical and structural properties. These devices had very high values of BV_{CEO} and consequently very thick epitaxial layers. Therefore, one could conclude that those devices did not exhibit burnout for one of two reasons: either the applied V_{CE} was too low, or the ion penetration depth was not sufficient. There was nothing observed in the experiment to distinguish between the two; however, the result for each is the same. The i_B generated by the incident ion did not exceed the value of i_{BCrit} given by the feedback mechanism which forced the currents within the device to decay to zero. Two of the three device types (2N3902 and 2N3055) that did not burnout follow this reasoning. The 2N3902 had a measured BV_{CEO} between 650V and 830V. Since the maximum voltage allowed with the experimental set up was 334V, the applied voltage was probably too low to induce burnout. The 2N3055 had an emitter diffusion depth of about 61μm. Since the largest penetration depth was 42μm, the ion did not even penetrate through the emitter region; therefore, the BJT was never turned on. These devices may have exhibited burnout behavior if the penetration depth or the collector voltage was increased.

The behavior of the final two devices (2NXXXX and 2N6284) can be explained from their electrical characteristics and layout. The first device, 2NXXXX, an experimental part that incorporated specific process and design techniques that should have prevented burnout from occurring. Recall that the magnitude of internal base resistance is a key parameter in the feedback mechanism for burnout. As the resistance is increased, the burnout susceptibility of the power BJT is increased. The resistance in the base region is directly proportional to the emitter stripe width, w_E. The wider the emitter stripe is the farther the lateral base current must travel before ground is reached, and hence the larger the internal base resistance is. The Gummel number is a measure of the areal doping density in the base region and is obtained by measuring the intercept current of the BJT [13]. The base resistance is inversely proportional to the Gummel number (ie., the higher the base doping, the lower the resistance).
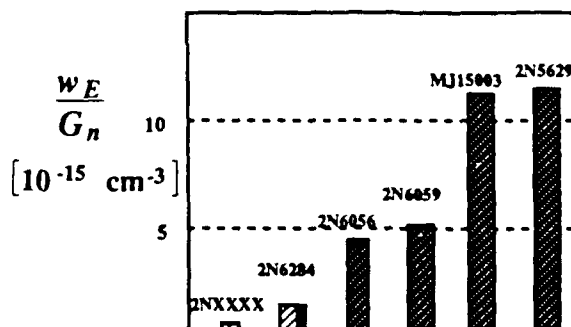

Figure 12: Ratio of emitter width to Gummel number.

Therefore a measure of the resistance in the lateral base region can be obtained by dividing the emitter width by the Gummel number. A plot of this ratio for six of the device types is shown in Figure 12. Notice that the 2NXXXX, which never exhibited burnout behavior, has the lowest base resistance. The 2N6284, which exhibited burnout for only one part in seven, has the next lowest base resistance. The two Darlington pairs, 2N6056 and 2N6059, have similar base resistances and had similar burnout susceptibilities. The two single devices which exhibited burnout, 2N5629 and MJ15003, have similar base resistances and had similar burnout susceptibilities.

V. SUMMARY AND CONCLUSIONS

Single-event burnout of power BJTs biased lower than their measured BV_{CEO} has been experimentally verified and reported for the first time. A model of the burnout mechanism, similar to the model used for power MOSFETs, helped explain the test results and the susceptibility of the devices. Burnout susceptibility was increased by increasing the internal base resistance. Reducing the emitter-stripe width proved to be a feasible design method to fabricate more robust power BJTs with respect to heavy-ion induced burnout.

VI. ACKNOWLEDGEMENTS

The authors would like to express their sincere thanks to the failure analysis group at the Naval Weapons Support Center with special thanks to Fred Barsun, Mark Helms, and Elvin Jones. The authors would also like to express their sincere thanks to Jakob Hohl for his technical insight of the problem and to LCDR Lewis Cohn, Dale Platteter, and Dave Emily for their interest in this work.

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IV.   Simulation of the Effect of Ionizing Radiation on Power-MOSFET Breakdown Voltage

IV.A   Introduction

The goal of this project was to develop a tool for simulating the performance of power-MOSFET termination structures in total-ionizing-dose environments. The simulation code that was developed is entitled ASEPS (Arizona SEmiconductor Power device Simulator). ASEPS is a two-dimensional code that solves Poisson's equation for reverse-biased junctions, using the assumption that there is no current flowing in the device. The advantages of ASEPS are short simulation times compared to general purpose device simulation tools and simple inclusion of radiation-induced charge densities.

A PC-based version of the ASEPS code has been completed and is available to DNA personnel. The software has been provided to Harris-Mountaintop, along with a simplified set of instructions and examples.

In addition to development of the software, the code has been used to simulate termination structures including field plates, floating rings, and novel 2,000-V termination structures for Motorola SPS. Additional work to examine charge buildup in field oxides using ASEPS is discussed in Section V below. The results of using ASEPS to simulate termination structures are described in detail in three publications. The papers are included in Sections IV.B–IV.D. A brief overview of each paper is included here to guide the reader through this material. Section IV.E includes users instructions and examples for ASEPS.

Section IV.B: K.R. Davis, R.D. Schrimpf, F.E. Cellier, K.F. Galloway, D.I. Burton, and C.F. Wheatley Jr., "Effects of Ionizing Radiation on Power MOSFET Termination Structures," *IEEE Trans. Nucl. Sci.*, vol. NS-36, pp. 2104-2109, 1989.

> In this paper, the degradation of breakdown voltage in n-channel power MOSFETs is examined. It is shown that field rings are less sensitive to a given amount of radiation-induced charge than are field plates.

Section IV.C: S.L. Kosier, R.D. Schrimpf, F.E. Cellier, and K.F. Galloway, "The Effects of Ionizing Radiation on the Breakdown Voltage of P-Channel Power MOSFETs," *IEEE Trans. Nucl. Sci.*, vol. NS-37, pp. 2076-2082, 1990.

> It is shown that p-channel power MOSFETs may exhibit an increase in breakdown voltage with total dose. This is caused by increased spreading of the depletion region due to the positive oxide charge. It may cause problems if the potential drop extends out to the edge of the chip or device isolation area.

Section IV.D: S.L. Kosier, D. Zupac, R.D. Schrimpf, F.E. Cellier, K.F. Galloway, M.N. Darwish, C.A. Goodwin, and M.C. Dolly, "Optimization of a Two-Level Field-Plate Termination Structure for Integrated-Power Applications in Ionizing Radiation Environments," in *Government Microcircuit Applications Conference Digest of Papers*, 1990, pp. 435-438.

The predictions of ASEPS are compared to experimental results for a specific termination structure. Design of an optimized structure is discussed.

IV.B Effects of Ionizing Radiation on Power-MOSFET Termination Structures

THE EFFECTS OF IONIZING RADIATION ON
POWER-MOSFET TERMINATION STRUCTURES*

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ABSTRACT

The effects of ionizing radiation on power-MOSFET termination structures were examined through two-dimensional simulation. A wide range of sensitivity to surface-charge density was found for various devices employing floating field rings and/or equipotential field plates. Termination structures that were both insensitive to surface charge and possessed a high breakdown voltage were identified. The results were compared with measurements made on selected structures.

I. INTRODUCTION

The maximum breakdown voltage obtainable for a p-n junction of specified doping concentration occurs for a planar structure [1]. In actual devices utilizing planar diffusion technology, however, the high-voltage junction must intersect the surface at some finite position. The resulting junction curvature compresses the equipotential lines where the junction bends to the surface and increases the peak electric field. Junction-termination structures are used in power devices to reduce the peak electric field and to allow the breakdown voltage to approach its ideal one-dimensional value. The most commonly used termination methods are field rings and field plates.

Avalanche multiplication is the physical mechanism that causes the primary breakdown of high-voltage reverse-biased p-n junctions. Breakdown occurs when the electric field in the junction depletion region increases to the point at which the impact ionization rate approaches infinity. The most important factor that influences the magnitude and location of the peak electric field in planar semiconductor technology is the method used to terminate the junction [1-3]. The objective of the different termination methods is to reduce the peak electric field either at the surface or at the curved junction regions in the bulk.

The drain-source breakdown voltage of power MOSFETs

is strongly affected by ionizing radiation [4, 5]. This is a result of the introduction of trapped oxide and interface charge in the field oxide. These trapped charges alter the potential at the surface of the junction and, in turn, become a part of the junction termination. Therefore, radiation-induced charge affects the breakdown voltage of high-voltage junctions.

This paper reports on work designed to examine the effects of ionizing radiation on the most commonly used power-MOSFET termination structures. Simulations were conducted using computer code specifically designed for this purpose. The results are presented and verified with measurements made on selected structures. Insights into the design of optimum termination structures are obtained.

II. HIGH-VOLTAGE TERMINATION TECHNIQUES

Junction curvature significantly reduces the breakdown voltage of p-n junctions because of the increase of the electric field in the curved area [1]. This curvature is dependent on the junction depth, the ratio of the radius of curvature to depletion width, and the relative doping concentration. High-voltage devices rely on the minimization of this curvature through the use of appropriate junction termination structures.

A. Floating Field Rings

Figure 1 shows the cross-section of a power-MOSFET which includes one floating field ring. Field rings are often used to reduce the electric-field magnitude in the vicinity of the curved regions of the junction. The structure is designed
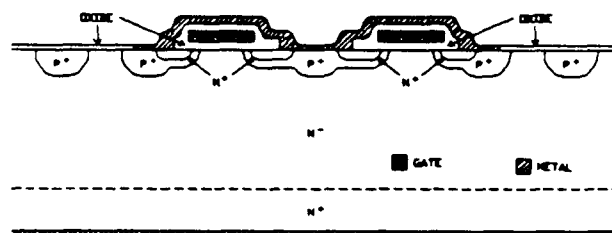

Fig. 1   Cross-section of power MOSFET with one floating field ring.

to allow the reverse-biased junction's depletion region to punch-through to the ring well before the critical electric field for breakdown is attained. The effectiveness of the floating field ring is the greatest for high-voltage devices fabricated with shallow junctions [3]. When no surface charge is present, punch-through occurs at the surface. With the addition of surface charge, the depletion region may be compressed at the surface. In this case, for the field ring to be effective, punch-through must take place in the bulk silicon before the surface electric field becomes so high that breakdown occurs.

Optimally placing the field ring can result in a doubling of the breakdown voltage [7]. This optimal spacing depends on the oxide thickness and doping concentration. Adding surface charge in N-channel power-MOSFETs decreases the breakdown voltage [4, 5]. When the surface charge is fixed, it is possible to determine the optimal location of the field ring. 'Vhen the surface charge is varied, however, the optimal location of the field ring changes, also.

B. Equipotential Field Plates

A field plate is a conductor placed above, and insulated from, the junction. It is usually connected to one side of the junction and is an extension of the junction metallization over the oxide as shown in Fig. 2. A field plate alters the surface potential by acting through the oxide layer to force the depletion layer at the surface to extend beyond the edge of the field plate. This "stretching out" of the depletion region reduces the depletion layer curvature and, in turn, reduces the peak electric field. It is common to use a field plate in conjunction with floating field rings by placing the plate on the main junction with floating rings beyond the junction or using a field plate on the last floating ring as shown in Fig. 3.
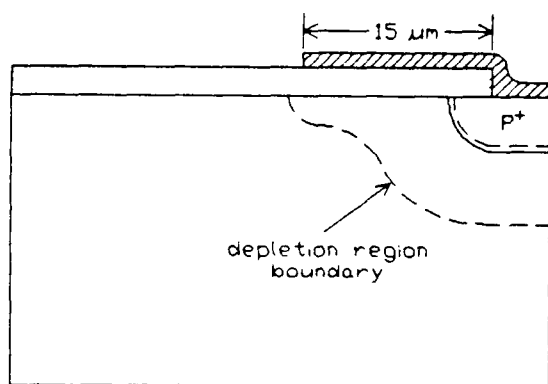

Fig. 2   Field-plate termination structure (After Baliga [3]).

III. METHOD OF SIMULATION

Computer code designed to analyze breakdown phenomena in high-voltage devices [6] has been modified to
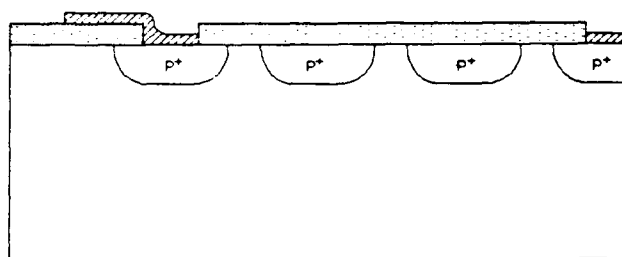

Fig. 3   Termination structure using combination of field rings and field plates. (After Baliga [3]).

simulate the effects of ionizing radiation on the breakdown voltage of power-MOSFETs. The code, entitled ASEPS (Arizona SEmiconductor Power device Simulator), solves Poisson's equation for the electrostatic potential distribution in two dimensions for an arbitrary device, subject to appropriate boundary conditions.   Unlike many general-purpose simulators, ASEPS neglects the contribution of mobile charge to Poisson's equation. This approximation is very accurate for strongly reverse-biased junctions. This simplification results in reduced simulation time and improved convergence of the solution, without significant sacrifice in accuracy. Average simulation times on a Digital Equipment Corporation MicroVAX 3600 range from 5 minutes for simple structures to 25 minutes for more complex structures. ASEPS interfaces with AutoCAD [13] to produce detailed drawings of the potential distribution and electric field distribution suitable for analysis.

The radiation-induced areal surface-charge density, N_{ss}, used in the difference equations is an input parameter to the ASEPS code. In this work, N_{ss} represents the algebraic difference between the positive oxide trapped charge (N_{ot}) and the negative interface trapped charge (N_{it}) and is taken to be positive. ASEPS draws a rectangular box around each node of the discretized domain of the structure being simulated, and this surface-charge density is only included in the difference equations for those nodes at the surface. A 200 × 200 grid is practical for describing the simulation domain of the structure. The Newton successive overrelaxation method of solving the resulting nonlinear equations is employed until convergence of a solution is reached.

ASEPS uses the ionization integral,

$$1 - \frac{1}{M_p} = \int_0^x \alpha_p \, exp\left[\int_0^{x'} \left(\alpha_n - \alpha_p \right) dx'' \right] dx' \qquad (1)$$

to calculate the multiplication factor for determination of avalanche breakdown [7]. In Eq. 1, M_p is the multiplication factor for holes, α_p is the ionization rate for holes, α_n is the ionization rate for electrons, and x is the depletion-layer

width of the ionization path. The ionization path is determined by starting from the peak electric field location and following the potential gradient line in both directions [8]. Ionization rates are from Sze and Gibbons [9]. Breakdown was assumed to occur when the multiplication factor for holes, M_p, reached the value of 10 [10].

IV. RESULTS

For a one-dimensional abrupt junction, breakdown voltage is approximated by the following equation [7],

$$V_{BD} = \frac{\varepsilon E_{max}^2}{2 q N_{BC}},\qquad(2)$$

where ε is the permittivity, E_{max} is the maximum electric field, q is the elementary charge, and N_{BC} is the background (substrate) doping concentration. A one-dimensional structure was simulated using ASEPS. The doping profile used was approximately Gaussian with a surface concentration of 1×10^{18} cm^{-3}. The substrate concentration was approximately 0.9×10^{15} cm^{-3}. This doping profile was obtained from spreading resistance measurements made on an existent device. ASEPS calculated the breakdown voltage to be 327 V with an E_{max} of 3.0×10^5 V/cm, while Eq. (2) predicts that the breakdown voltage will be 324 V. Thus for this simple example, there is less than a 1% difference between Eq. (2) and simulation.

A simple p-n junction formed by diffusion is considered next. Fig. 4a shows a cross section of this structure with equipotential lines calculated by ASEPS superimposed. The junction depth is 5 μm, the oxide thickness is 0.7 μm, N_{ss} is zero, and the doping profile described above is used. The solid circle in Fig. 4a shows the location of the peak electric field. The value of the field is 3.5×10^5 V/cm. Calculation of the multiplication factor along the ionization path indicated that breakdown occurred for a reverse-bias voltage of 194 V. 194 V is only 59% of the optimal 327 V that might be achieved in an ideal junction with $N_{BC} = 0.9 \times 10^{15}$ cm^{-3}.

Fig. 4b shows the same cross section except that the device was simulated with $N_{ss} = 1 \times 10^{12}$ charges/cm^2. Because the net charge in the oxide has been taken to be positive, the carrier density in the n$^-$ region near the surface increases. This causes a decrease in depletion layer width and the crowding of the potential lines at the surface. The solid circle, again, shows the peak electric field location, which has moved to the surface. This location of the peak electric field results in a drastic reduction in breakdown voltage. A plot of breakdown voltage versus surface-charge density for this device can be found as the curve labeled "0 Rings" in Fig. 8.

The first technique considered to improve the breakdown voltage is the addition of one floating field ring optimally spaced from the main junction. This device, with the potential
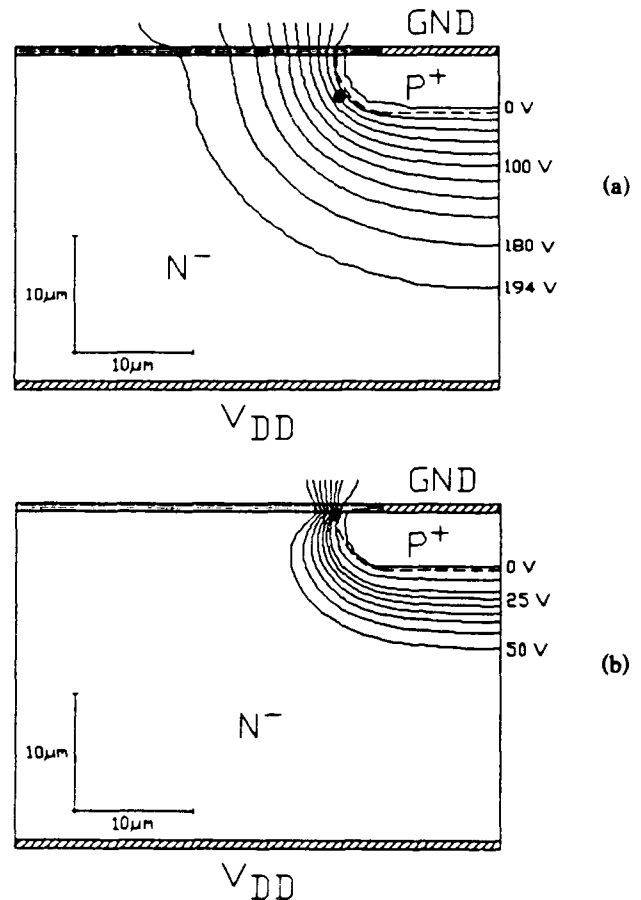

Fig. 4   Potential distribution for simple two-dimensional p-n junction. (a) $N_{ss} = 0$, $V_{BD} = 194$ V. (b) $N_{ss} = 10^{12}$ cm^{-2}, $V_{BD} = 92$ V.

distribution for $N_{ss} = 0$, is shown in Fig. 5 where optimal spacing is achieved because the high electric field spots (circles) appear on both junction curvatures simultaneously indicating that both junctions broke down. From the computer simulations, it was verified that this spacing resulted in the highest breakdown voltage. This optimal spacing was 9.5 μm
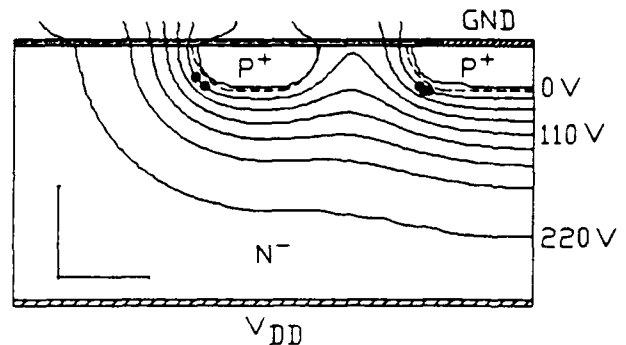

Fig. 5   Potential distribution for one-ring termination structure ($N_{ss} = 0$, $V_{BD} = 250$ V).

between rings after lateral diffusion. Figure 8, where breakdown voltage of this one-ring device is plotted versus surface charge, indicates that for N_{ss} = 9 × 10^{11} cm^{-2} or greater, the breakdown curve followed that of the zero-ring device. This happened because punch-through to the field ring did not take place before breakdown occurred at this value of N_{ss}. Better results were obtained for a three-ring device. Again, the sharp bends in the curve plotted in Fig. 8 are a result of the punch-through phenomenon not reaching a ring before breakdown occurred. The spacing of the rings was kept fixed in determining the optimal spacing in this three-ring device. It was found that this distance was 7.5 μm and this device structure is shown in Fig. 6, with the overlaid potential distribution simulated for N_{ss} = 0.
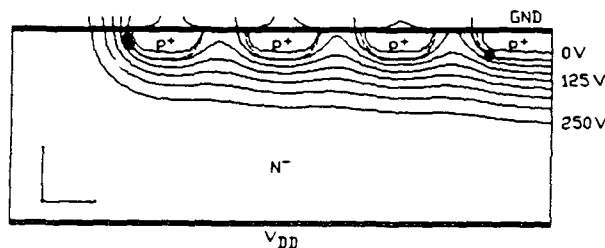

Fig. 6 Potential distribution for three-ring termination structure (N_{ss} = 0, V_{BD} = 278 V).

Variable ring spacing increases the breakdown voltage of devices having more than one ring. For avalanche breakdown to occur on all rings simultaneously, the spacing between different pairs of rings must be non-constant. The seven-ring breakdown curve in Fig. 8 is for a device with this type of spacing. Fig. 7 shows this device, with the potential distribution for N_{ss} = 0, where the spacing between the first ring and the main junction is 2.0 μm, increasing to 12.0 μm between the last pair of rings. Experimental measurements on this device indicated no degradation of the 268 V breakdown voltage for total-dose levels up to 1 MRad(Si). ASEPS calcu-

lated the breakdown voltage to be 281 V which is in error by only 5%. From the potential distribution in Fig. 7, it can be seen that the depletion layer depth below each ring gradually decreases as one moves farther from the main junction. The potential difference between a ring and the bulk material decreases as the distance of the ring from the main junction increases. This gradual decrease in depletion layer depth causes the termination to approximate the performance of a parallel-plane junction.

The measured breakdown voltage of a six-ring structure is plotted versus surface-charge density in Fig. 9. Each data point represents the average of six samples. The total dose has been converted to surface-charge density using the formula [12],

$$N_{ss} = D t_{ox} G F \qquad (3)$$

where D is the total dose, t_{ox} is the oxide thickness, G is the generation rate of electron-hole pairs per unit volume, and F is the fraction of holes transported and trapped at the interface. An appropriate value of F was used in this simple model (F = 0.001) to calibrate the experimental data to the simulation. A more sophisticated model or additional experiments could be used to establish more precisely the relation between total dose and surface-charge density if required. In most situations, however, it is sufficient to minimize the dependence of breakdown voltage on surface-charge density.

The field plate/field ring combination shown in Fig. 10a had an initial breakdown voltage that was higher than that of a one-ring structure, but the advantage disappeared with increased surface charge. This is due to the fact that punch-through does not occur for higher charge densities and the plate has no effect (Fig. 10b). These results are presented in Fig. 11 where a comparison of this plate structure is made with the one-ring structure that does not use a field plate.
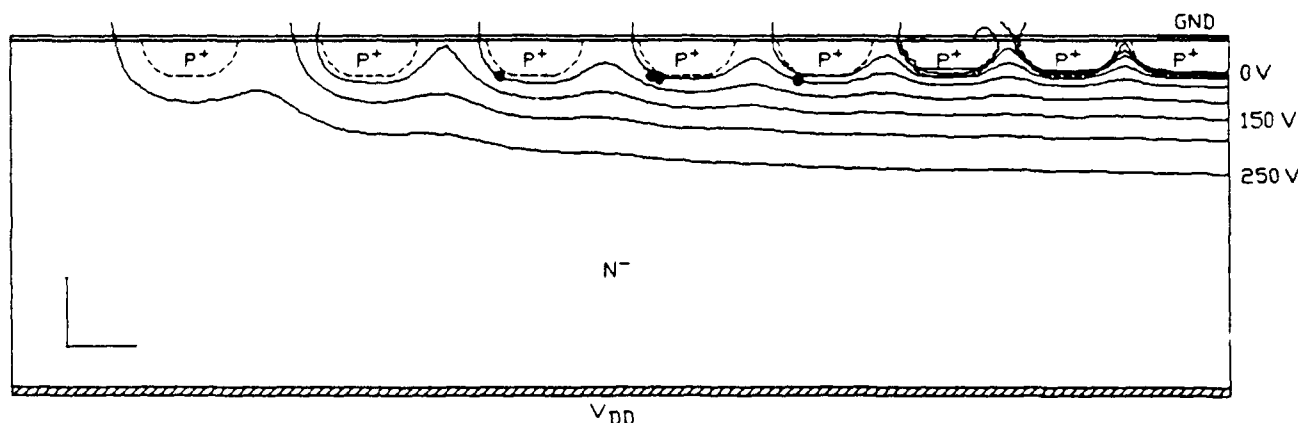

Fig. 7 Potential distribution for seven-ring termination structure (N_{ss} = 0, V_{BD} = 281 V).
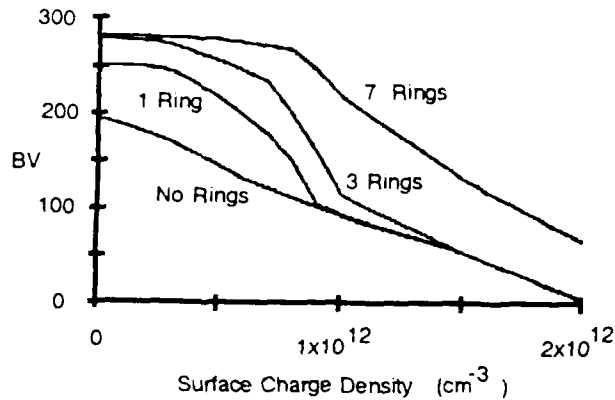
Fig. 8 Breakdown voltage vs. surface-charge density for various numbers of floating rings.

V. CONCLUSIONS

The breakdown behavior of typical power-MOSFET termination structures was examined as a function of radiation-induced surface charge, and the results for selected structures were verified experimentally. The specific results presented are a function of doping profile and oxide thickness, but the approach is readily applicable to structures with other values of these parameters. A wide range of sensitivity to radiation-induced charge was found for different termination structures.

For a field plate to be effective in increasing the breakdown voltage, it is necessary to use an oxide thickness sufficiently large so that the depletion layer curvature is reduced and the peak electric field is moved lower in the semiconductor bulk. With a large oxide thickness, though, the structure is very sensitive to surface charge. This causes field-plate terminations to degrade severely in radiation environments because field plates modify the potential distribution in the semiconductor by acting through an intervening dielectric layer. Any charge that is added in this dielectric layer produces a significant change in the potential distribution in the semiconductor.
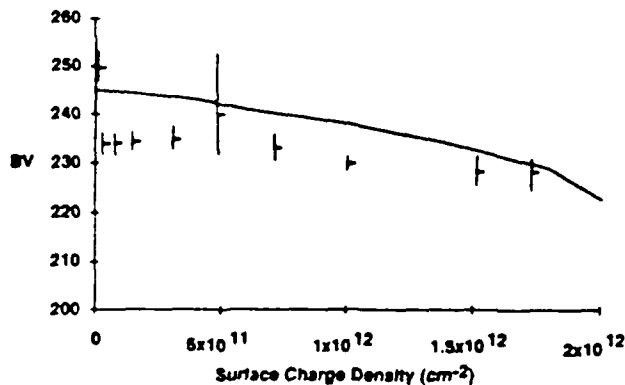

Fig. 9 Breakdown voltage vs. surface-charge density for a six-ring structure. Each data point represents the average of six samples. The line represents simulation results.

To achieve a high breakdown voltage and low sensitivity to surface charge, a device employing multiple field rings was found to work well. With just one ring, the breakdown voltage was substantially increased and sensitivity to surface charge was reduced. The optimal spacing of this ring was found to be 9.5 µm such that the breakdown voltage was maximized and the peak electric field minimized for the given impurity profile. The optimal spacing of a three-ring device was 7.5 µm between rings spaced uniformly. For avalanche multiplication to occur on all rings simultaneously, the spacing of the rings should gradually increase as distance from the main junction increases. This method of spacing the rings was used in the seven-ring device where the first ring was spaced 2.0 µm from the main junction.
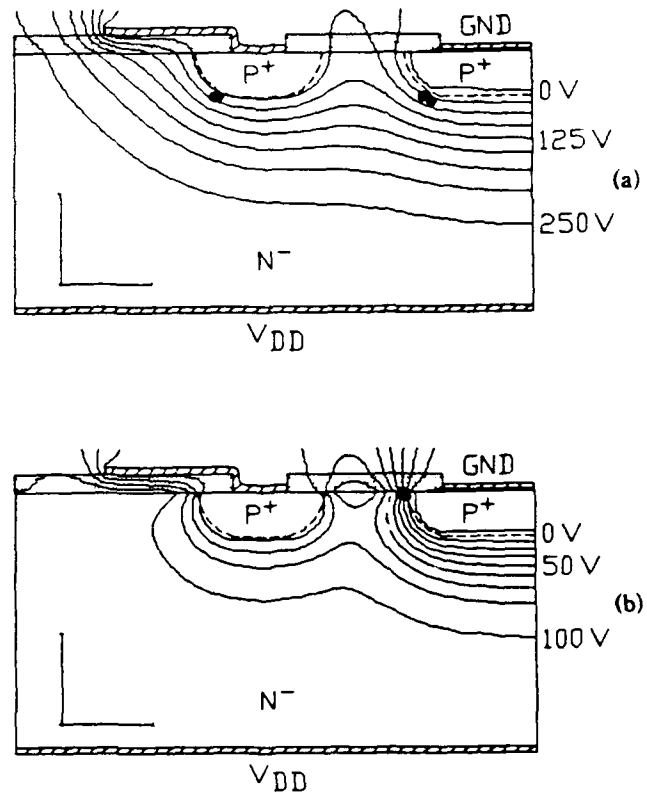

Fig. 10 Potential distribution for combination ring/plate structure. (a) N_{ss} = 0, V_{BD} = 270 V. (b) N_{ss} = 10^{12} cm^{-3}, V_{BD} = 92 V.

The trend is that as the number of rings in the device is increased, the spacing between these rings should steadily decrease. The best results are obtained for devices with a large number of rings and very little spacing between them.

There is, however, a tradeoff between die area and the desired increase in breakdown voltage and the desired insensitivity to surface charge. The increase in breakdown voltage of an eight-ring device over a seven-ring device is very slight. The most appropriate number of rings will be de-
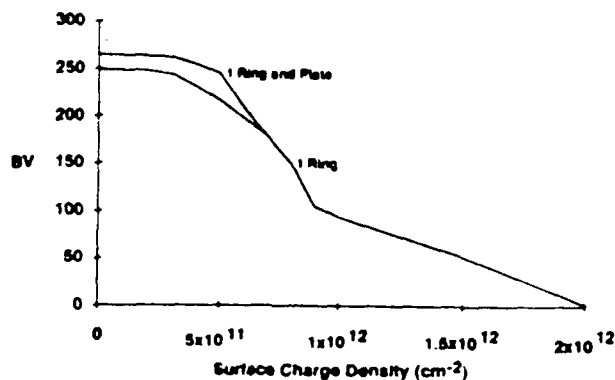
Fig. 11 Breakdown voltage vs. surface charge density for a one-ring structure and a one-ring structure with a field plate.

termined by the application and by the radiation environment in which the device is to be deployed.

Great care must be taken when designing a power MOSFET for use in an ionizing radiation environment. ASEPS has proven to be a valuable tool for this type of design work [14]. Of the structures examined, multiple floating rings had the least sensitivity to radiation-induced charge. The spacing between these rings is critical because radiation-induced charge can render the outer rings ineffective if the distance between them is too large. By using ASEPS with some initial insight as to what the spacing should be, one has a good starting point for determining optimal ring spacing.

VI. ACKNOWLEDGEMENTS

We would like to express thanks to Burr-Brown Corporation for the use of computer resources and an early involvement in the development of the ASEPS code. Also, we would like to thank Chi-min Yen and Leonghin Tan for their contributions to the development of the original code. Finally, we appreciate the interest of Tom Ellis, Jeff Titus, Dale Platteter, and Lew Cohn in this problem.

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IV.C The Effects of Ionizing Radiation on the Breakdown Voltage of *P*-Channel Power MOSFETs

THE EFFECTS OF IONIZING RADIATION ON THE BREAKDOWN VOLTAGE OF P-CHANNEL POWER MOSFETS†

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ABSTRACT

The effects of ionizing radiation on the breakdown voltage of p-channel power MOSFETs were examined through two-dimensional simulation. Breakdown-voltage performance of p-channel power MOSFETs was found to be very different from corresponding n-channel power MOSFETs. In p-channel devices, simulation showed breakdown-voltage enhancement for low values of positive oxide-trapped charge, N_{ot}, whereas for high values of N_{ot}, the breakdown voltage may or may not continue to increase, and may actually decrease in some topologies. For comparison, in n-channel devices, increases in N_{ot} always cause breakdown-voltage degradation. The uncertainties stem from the interaction of the depletion region of the device (which is a function of its termination method) with its isolation technology, making it difficult to predict breakdown voltage for large N_{ot}. However, insights gained through analysis of depletion-region spreading in p-channel devices suggest a termination/isolation scheme, the VLD-FRR, that will enhance p-channel device reliability in radiation environments.

I. INTRODUCTION

P-channel power MOSFETs are of potential value for applications in radiation environments. It has been suggested that p-channel DMOS devices typically are less sensitive to gamma-dot [1] and single-event burnout [2], and may have a smaller threshold-voltage shift than n-channel devices under typical bias conditions [3]. When either an n- or a p-channel device can be used in a circuit, these advantages may offset the disadvantage of higher on-resistance of the p-channel device. For applications that require complementary drivers [4], such as power amplifiers with complementary output stages, rad-hard p-channel devices would be extremely useful, since complementary devices greatly simplify gate-drive circuit design.

One parameter that is not yet well understood for p-channel power MOSFETs, and thus makes design of rad-hard p-channel devices difficult, is the dependence of drain-source breakdown voltage on ionizing radiation. It is often tacitly assumed that p-channel device breakdown voltage will increase, and surely not degrade, in an ionizing radiation environment. Earlier research has supported this assumption [5].

P-channel devices usually employ the same termination topology, and, if integrated, the same isolation technology, as n-channel devices of similar voltage rating. Thus, their pre-rad breakdown voltages are practically identical for complementary doping and topology. As will be demonstrated in this paper, using identical termination structure topology and isolation technology for n- and p-channel devices is not always warranted. This is because of the fundamentally different effects ionizing radiation has on the spreading of the drain-body depletion region of the two device types.

II. SIMULATION METHOD

Computer code designed to simulate the effects of ionizing radiation on the breakdown voltage of power semiconductor devices has been developed at the University of Arizona [6, 7]. The code, entitled ASEPS (Arizona SEmiconductor Power device Simulator), solves Poisson's equation in two dimensions. Breakdown voltage is then determined by computing the ionization integral through the locus of highest-field points at every potential. ASEPS has proven to be an accurate and efficient simulator of highly reverse-biased junctions with arbitrary termination topologies and varying amounts of radiation-induced oxide charge [6, 7]. Its flexible input format enables comprehensive study of competing termination designs.

III. TERMINATION STRUCTURES

The primary goal of a termination structure is to raise the breakdown voltage of a planar p-n junction to its maximum, or parallel-plane, value [8]. Termination structures do this by countering the effects of p-n junction curvature that arise in planar processing. In power MOSFETs, the drain-body p-n junction limits the breakdown-voltage performance of the device; thus termination structures are built for this junction alone.

For rad-hard devices, an equally important task for the termination structure is the retention of the pre-irradiation breakdown voltage, even at high values of radiation-induced positive oxide-trapped charge, N_{ot}.

Various methods of junction termination have been proposed and implemented, but the two most frequently used methods are field plates (FPs) and field-limiting rings (FLRs) [6, 7, 8]. FLR termination structures rely on the punchthrough mechanism to decrease the effects of junction curvature [9], while FP termination structures make use of the total bias voltage, V_{tot}, to induce charges in the device that effectively extend the junction they are terminating [10].

IV. INVESTIGATION APPROACH

A. Parameters

To demonstrate the similarities and differences between n- and p-channel power MOSFET breakdown voltage behavior, three different devices were simulated over a wide range of radiation-induced oxide charge. Data for each device are summarized in table 1. These values are representative of those found in typical low-, medium-, and high-voltage power integrated circuit (PIC) applications. In all ASEPS-generated figures in this paper, dark circles indicate highest-electric field points (which identify the part(s) of the device where breakdown occurs), and the lines are equipotential lines.

B. Modeling

In figures 1a and 1b, ASEPS simulation results for the drain-body junction belonging to the medium-voltage device of table 1 are shown with negligible N_{ot}. (Representative power-MOSFET cross-sections are shown in figure 3.) Note that figure 1a faithfully depicts either the outermost ring of an

Device Parameter

		Junction Depth [μm]	Substrate Doping [cm-3]	Parallel-Plane Vbreakdown [V]
Voltage Rating	low	3	1.1×10^{16}	50
	med	5	1.0×10^{15}	300
	high	40	2.0×10^{14}	1000

Table 1. Data for the devices discussed in the text and simulated with ASEPS.

$V_{tot} = \pm 165\ V$

n+ or p+

p or n

(a)

$V_{tot} = \pm 220\ V$

n+ or p+

p or n

(b)

$V_{tot} = -155\ V$

p+

n

(c)

$V_{top} = 200\ V$ $V_{tot} = 205\ V$

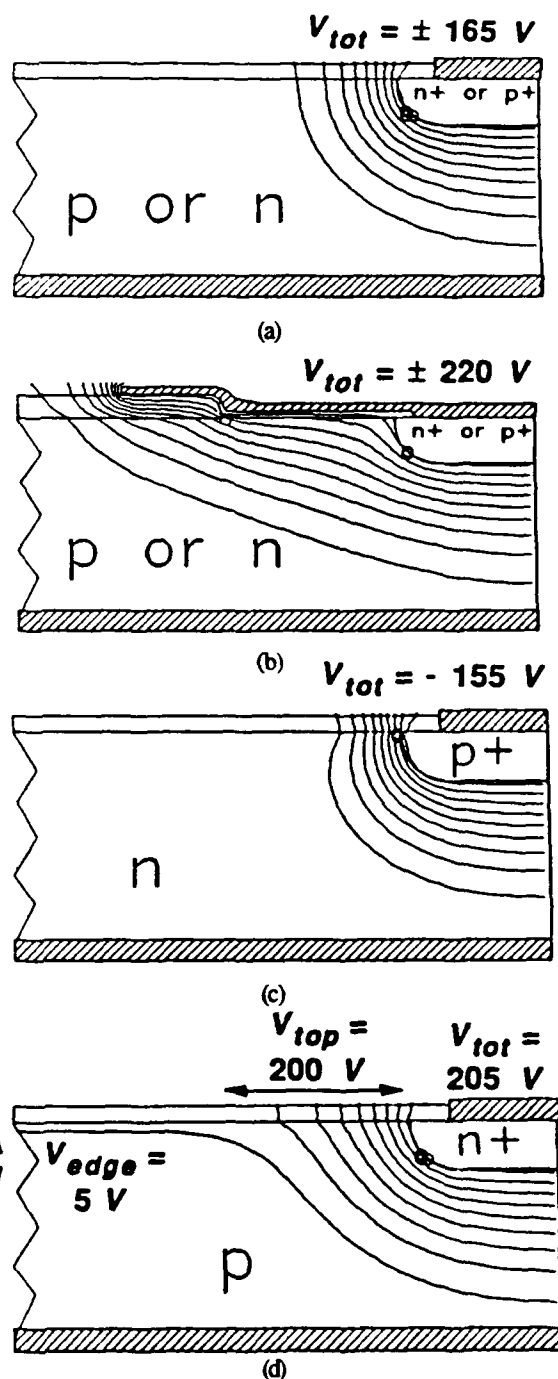$V_{edge} = 5\ V$

n+

p

(d)

Figure 1. ASEPS simulation results illustrating the different responses of n- and p-channel devices to N_{ot}. $V_{tot} = V_{break}$ in all figures. a) N- or p-channel device without termination and with negligible N_{ot}. b) N- or p-channel device with two-level field plate and negligible N_{ot}. c) N-channel device showing breakdown-voltage degradation with $N_{ot} = 3.0 \times 10^{11}\ cm^{-2}$. d) P-channel device showing breakdown-voltage enhancement with $N_{ot} = 3.0 \times 10^{11}\ cm^{-2}$, but V_{tot} is split between V_{top} and V_{edge}. This splitting can cause breakdown voltage degradation in some topologies.

FLR termination structure or an unterminated drain-body junction, while figure 1b shows an FP termination structure. The equipotential lines are distributed identically for both device polarities. Thus, any termination structure designed for an n-channel device will work equally well for a p-channel device of equal voltage rating, assuming negligible N_{ot}.

As N_{ot} increases, however, the breakdown performance of n- and p-channel devices diverges. Assuming N_{ot} is located at the Si-SiO$_2$ interface, the induced areal number density of semiconductor charge, N_s, is equal to N_{ot} due to simple electrostatics (i.e. $Q_s = -Q_{ot}$), regardless of device polarity. Thus, N_s serves to compress the equipotential lines in the n-channel device, which lowers breakdown voltage, as seen in figure 1c. A field plate will tend to offset this compression by inducing charge of opposite sign in the semiconductor. In the p-channel device, N_s effectively extends the main junction, decreasing the curvature of the equipotential lines and increasing the initial breakdown voltage, as seen in figure 1d. A field plate enhances this effect since both the plate-induced charge and the radiation-induced charge carry the same sign.

The breakdown voltage of the p-channel device may not increase indefinitely, however, as has often been assumed [5]. The reason can be understood by considering N_s in more detail. N_s resides in the silicon, and for large N_{ot}, most of it is confined to one extrinsic Debye length, L_D, of the Si-SiO$_2$ interface, where

$$L_D = \sqrt{\frac{\kappa_{Si}\,\varepsilon_0\,k\,T}{q^2\,N_{sub}}} \qquad (1)$$

In (1), κ_{Si} is the relative dielectric constant of silicon, ε_0 is the permittivity of free space, k is Boltzmann's constant, T is temperature in degrees Kelvin, q is the electronic charge, and N_{sub} is the substrate doping.

An effective n-type volumetric doping, valid within one L_D of the Si-SiO$_2$ interface, can be defined by $N_{eff} = N_s/L_D \approx N_{ot}/L_D$. (Detailed consideration of the charge profile in this region neither enhances accuracy nor aids physical understanding.) Once a certain critical value of surface charge, $N_{s,crit}$, is present, N_{eff} is sufficiently high that the entire depletion region cannot completely penetrate it. For $N_s > N_{s,crit}$, a fraction of the depletion region extends to the edge of the chip. Thus V_{tot} is divided between the top and the edge of the device, i.e. $V_{tot} = V_{top} + V_{edge}$, as indicated in figure 1d.

Intuitively, it is expected that as N_s increases beyond $N_{s,crit}$, V_{edge} will increase. In fact, simulation has shown that V_{top} and V_{edge} do not change simultaneously, and that V_{edge} has a maximum value for a given N_{ot}, $V_{edge}(max)$. That is, as

V_{tot} increases from $0\ V$ to some large positive voltage, V_{edge} increases from $0\ V$ to $V_{edge}\ (max)$, and then V_{top} increases from $0\ V$ to $V_{tot} - V_{edge}(max)$. $V_{edge}(max)$, then, is a function only of N_{ot} and N_{sub}.
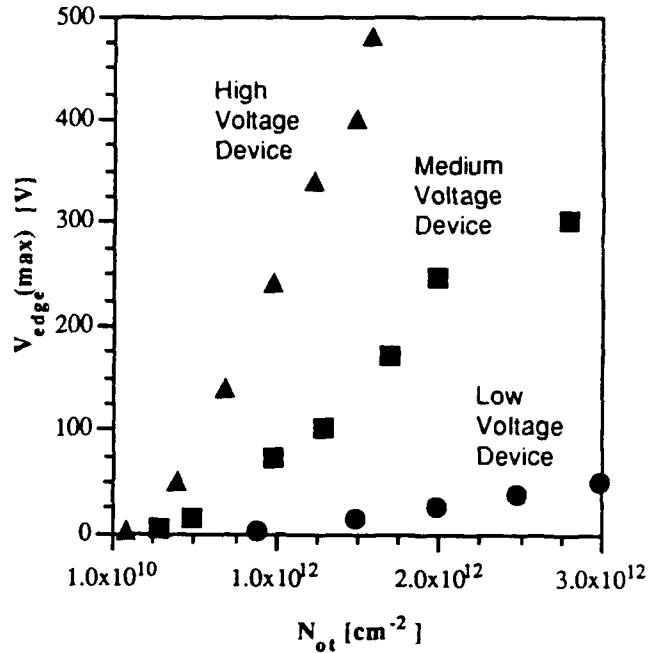

Figure 2. $V_{edge}(max)$ vs. N_{ot} for the three devices of table 1.

In figure 2, $V_{edge}(max)$ is plotted against N_{ot} for the three devices of table 1. In addition to the data displayed in figure 2, simulation has shown that $N_{eff} \approx 2\,N_{sub}$ defines $N_{s,crit}$ for any p-channel device, validating the previous assumptions about the charge distribution in the semiconductor.

Having established the characteristics and magnitude of V_{edge} a key result is obtained: although the p-channel breakdown voltage does legitimately increase for $N_s < N_{s,crit}$, assuming that it increases indefinitely presupposes that having $V_{edge} > 0$ does not degrade the breakdown voltage or circuit performance at all. This assumption is not justified. The V_{edge} component of V_{tot} can cause crosstalk, surface electric fields, and/or sharply reduced breakdown voltage, depending on the topology of the device under consideration.

V. IMPLICATIONS FOR TERMINATION STRUCTURES

Based on the results of section IV, the effectiveness of FP and FLR termination structures for p-channel devices in radiation environments can be predicted. For example, multiple-ring FLR termination structures may not be effective, since the punchthrough mechanism on which FLR designs rely is not intact for $N_s \geq N_{s,crit}$.

FP termination structures may be a better alternative for p-channel devices in radiation environments than are FLR designs. The reason, mentioned briefly in section IV, is that the presence of Q_{ot} enhances the effect of the FP. Quantitatively, an FP induces voltage-dependent areal charge in the substrate directly below the FP, Q_{plate}, where

$$Q_{plate} = \frac{K_{ox}\, \varepsilon_o}{t_{ox}} V_{tot} \quad , \qquad (2)$$

which carries the same algebraic sign (negative) as Q_s, giving $Q_s = Q_{plate} + Q_{ot}$. In (2), K_{ox} is the dielectic constant of silicon dioxide, ε_o is defined as in (1), and t_{ox} is the oxide thickness under the FP.
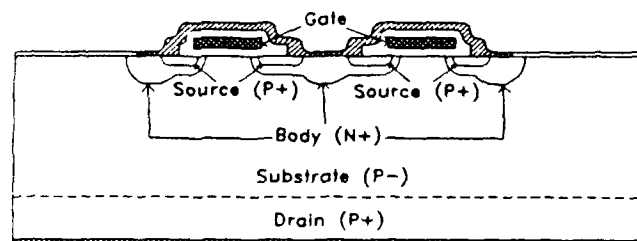
(a)
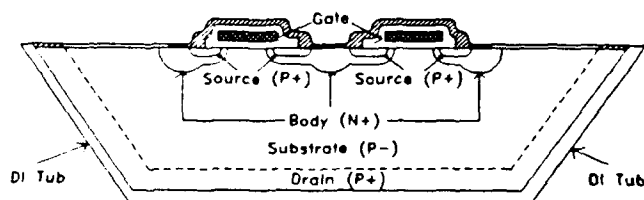
(b)

Figure 3. Types of p-channel power devices. a) Discrete device. b) Dielectrically-isolated integrated device.

The increase in Q_s under the FP for a given V_{tot} improves the breakdown voltage performance of the FP, since FP termination structures become more effective as N_{eff} increases beyond N_{sub}. The maximum breakdown voltage, obtainable for $N_{eff} \gg N_{sub}$, can be predicted from the device parameters N_{sub} and t_{ox} [11].

VI. IMPLICATIONS FOR DEVICE ISOLATION

Even with an FP termination structure, Q_{ot} still gives rise to V_{edge}, which now extends from the edge of the FP. So although the electric field near the FP termination structure itself will not cause device breakdown voltage to degrade, the electric field near the device isolation technology may. In fact, the actual termination structure, whether FPs, FLRs, or some other technique, does not influence the following discusion of device isolation, since all conventional termination structures will have a V_{edge} component that interacts with the device isolation. For the puposes of this discussion, then, assume that both $N_{ot} > N_{s,crit}$ and $V_{tot} > V_{edge(max)}$.

A. Discrete Power Devices

As seen in figure 3a, a discrete power device has its drain connection at the bottom of the wafer. If there is no isolation scheme to prevent the depletion region from spreading indefinitely, as is often the case, V_{edge} is dropped across the edge of the chip. This gives rise to surface electric fields, and thus unpredictable breakdown performance [12]. V_{edge} must be handled in this case by a beveled termination or some other surface passivation technique. Thus, a discrete p-channel power device should, at the very least, employ some sort of edge passivation and/or termination in addition to its existing termination structure if it is to be used in an ionizing radiation environment.

Beveled terminations are well understood [13], but are undesirable for a modem process. This is because they require a great deal more effort to realize than do planar terminations [14], and are incompatible with integrated power applications.

B. Integrated Power Devices

Two classes of integrated power devices are considered: junction-isolated and dielectrically-isolated (DI). A junction-isolated p-channel device can be particularly vulnerable to ionizing radiation, since V_{edge} could either punch through the isolation or simply extend (via its depletion layer) around the isolation and directly influence the logic circuitry. If this happens, it will almost certainly lead to system failure. If V_{edge} does not punch through or go under the isolation, junction isolation is as effective as dielectric isolation.

At first glance, DI p-channel power devices may seem impervious to ionizing radiation, since the p+ wraparound (the drain contact in figure 3b) forces the depletion layer of V_{edge} through the top of the device. When sufficient N_{ot} is present, however, the breakdown voltage of a DI device will drop precipitously, far below its pre-rad value. The reason is that equipotential crowding, and thus device breakdown, occurs at the intersection of the drain contact with the surface.

To demonstrate this phenomenon, the three devices of table 1 were simulated in DI tubs without any termination structures and their breakdown voltage, V_{break}, vs. N_{ot} was obtained. A representative result is displayed in figure 4a. In figure 4b, ΔV_{break} is plotted vs. N_{ot} for all three devices. The value of
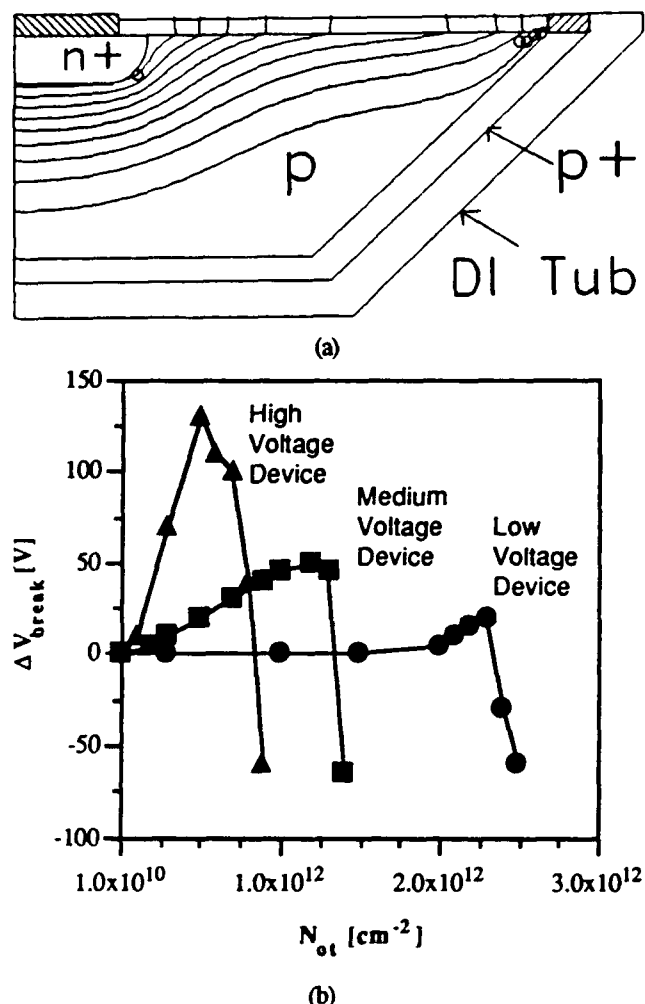
(a)

(b)

Figure 4. Radiation-induced breakdown in integrated p-channel power devices. a) Medium voltage device of Table 1 with N_{ot} = 1.3×10^{12} cm⁻². V_{tot} = 215 V. b) ΔV_{break} vs. N_{ot} for all devices of table 1 in DI tubs.

N_{ot} for which sharp reductions in V_{break} first occur is inversely proportional to voltage rating.

In a real device, however, termination structures are always used. Consider the representative DI device of figure 5a, which is equipped with the two-level FP termination illustrated in figure 1b and described in the text of section IV.B. There are two cross-sections of interest in figure 5a, O – A and O – B. Through O – A, breakdown voltage degradation occurs for smaller N_{ot} than through O – B. This is because the source contact acts as a "parasitic FP", inducing N_{plate} along its entire length, which causes $N_{s,crit}$ to be reached for lower values of N_{ot} than through O – B. A cross-section through O – A illustrating this effect is shown in figure 5b. In figure 5c, ΔV_{break} versus N_{ot} is plotted for this
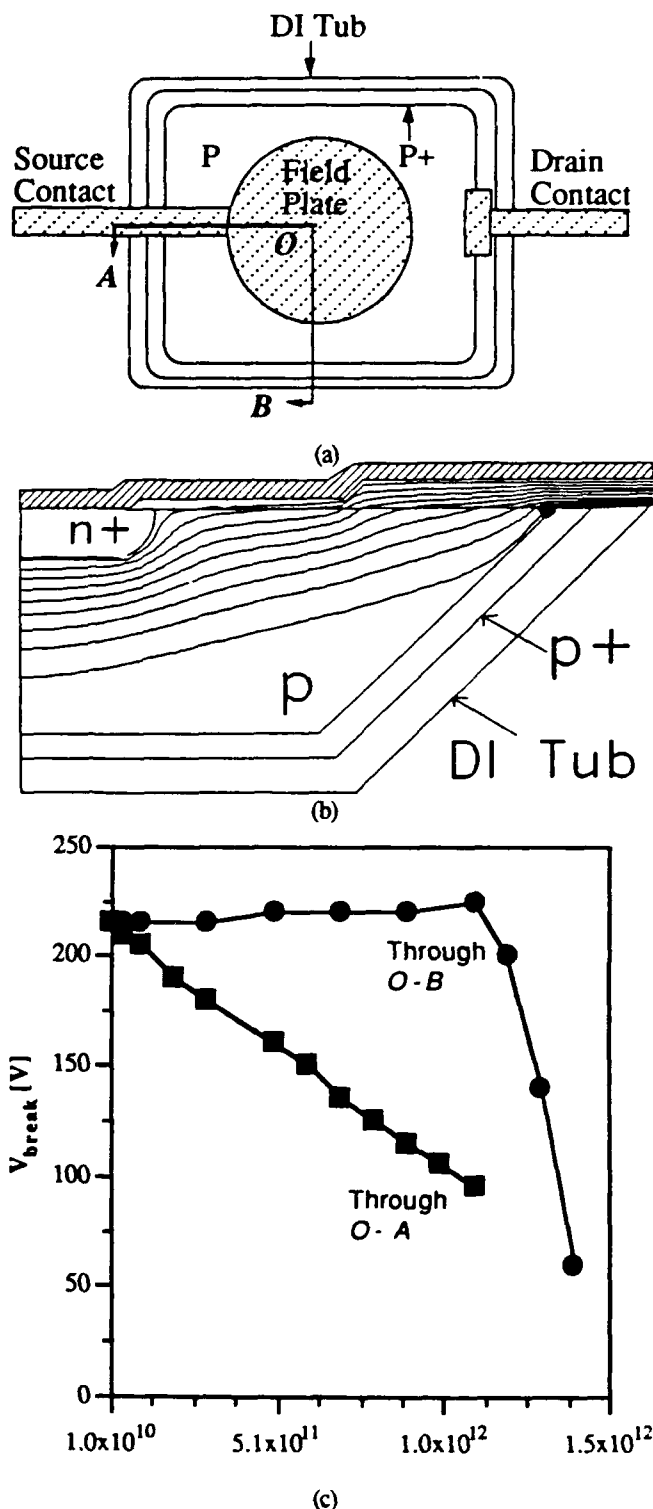

(a)

(b)

(c)

Figure 5. Medium voltage device of Table 1 in a realistic DI application. a) Top view of device. b) Cross section though O – A, demonstrating deleterious effects of the source contact. V_{tot} = 190 V. N_{ot} = 2×10^{11} cm⁻². c) Breakdown voltage vs. N_{ot} for O – A and O – B cross-sections.

device through both cross-sections $O - A$ and $O - B$, indicating that the $O - A$ cross-section limits the breakdown perfomance of the DI device, as has been reported elsewhere [15].

It is of interest to note that the phenomenon described above is not restricted to p-channel power device applications. The analogy between this case and that of a negative power supply line over a p-tub in a CMOS application, for instance, is apparent.

C. General Observations

Ionizing radiation can degrade the performance of all p-channel power devices. The degradation, which depends strongly on the termination structure and isolation technology of the device, is a direct result of the spreading of the depletion region beyond its pre-rad boundary via V_{edge}. It follows that V_{edge} must be controlled in an efficient p-channel termination/isolation scheme.
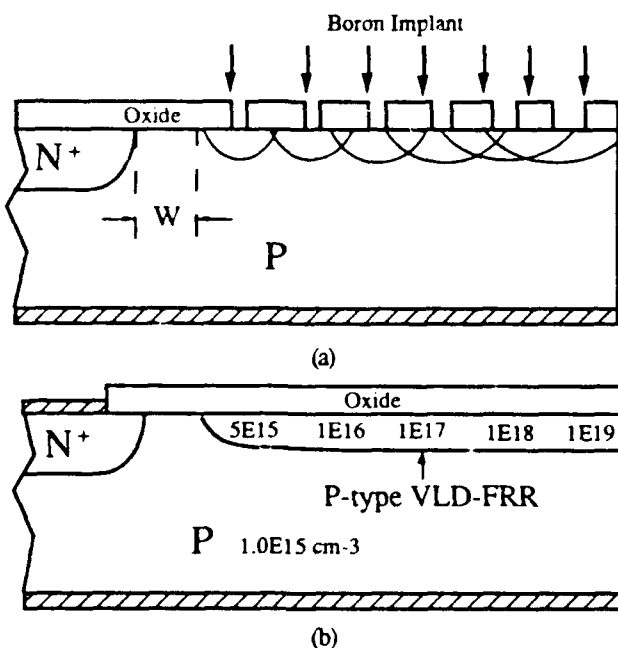

(a)

(b)

Figure 6. Conceptual illustration of the VLD-FRR. a) Ion implantation of boron takes place through specially-defined windows. The windows increase in thickness and decrease in spacing with lateral distance. W is the pre-rad depletion region width. b) A smoothly-varying VLD-FRR is obtained when boron diffuses in the anneal/drive-in step. The net positive charge in the VLD-FRR will compensate the radiation-induced negative charge, N_s, allowing redirection of the equipotential lines through the Si-SiO$_2$ interface without crowding.

VII. TERMINATION/ISOLATION STRATEGIES

In addition to the general statements about the goals of a termination structure outlined in section III, any rad-hard p-channel power device must meet two additional requirements: a) it must confine the depletion region to an acceptable region for all possible values of N_{ot}, and b) it must meet the breakdown voltage specification of the device for all possible values of N_{ot}. As a practical consideration, compatibility with standard planar processes is highly desirable.

In terms of previously defined variables, a method to redirect V_{edge} through the top of the device that avoids equipotential crowding for all values of N_{ot} is needed. To accomplish this task, a new type of termination/isolation technique is proposed: the VLD-FRR, which is an acronym for Variation of Lateral Doping–Field Reduction Region. The concept of a field-reduction region (FRR) has been described and implemented [15], and several ways of smoothly varying the lateral doping of an implant (VLD) for junction termination purposes have been described and implemented as well [16, 17, 18]. A combination of the two techniques will allow efficient redirection of V_{edge} through the device's surface.

The proposed fabrication method is illustrated qualitatively in figures 6a and 6b. This technique will work for integrated as well as discrete devices, and although it may represent an increase in device area, it ensures predictable and stable breakdown voltage for an extended range of N_{ot}. Proper selection of the implant dose, and the range of charge values (i.e., width and spacing of the windows), are, in general, device-specific. The obvious tradeoff is that of area versus performance; by using more lateral distance to vary the VLD-FRR's doping, improved breakdown performance can be expected.

VIII. CONCLUSION

Two-dimensional simulation has shown that n- and p-channel power-MOSFETs behave differently when exposed to ionizing radiation. These differences, which are not typically accounted for in the design of termination structures, can lead to poor breakdown performance of p-channel devices. The presence of V_{edge} for $N_{eff} > 2 N_{sub}$ has been demonstrated for all p-channel devices, and the implications of V_{edge} have been examined for FP and FLR termination structures, as well as for various isolation technologies. A VLD-FRR termination/isolation scheme is proposed to counter the effects of V_{edge} for all types of p-channel power devices in radiation environments.

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IV.D Optimization of a Two-Level Field-Plate Termination Structure for Integrated Power Applications in Ionizing Radiation Environments

OPTIMIZATION OF A TWO-LEVEL FIELD-PLATE TERMINATION STRUCTURE FOR INTEGRATED-POWER APPLICATIONS IN IONIZING RADIATION ENVIRONMENTS

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Abstract

Analysis of four two-level field plate (FP) termination structures for power-integrated circuit applications in ionizing radiation environments has been performed through two-dimensional simulation and experiment. Breakdown voltage degradation as a function of the distance the upper plate overlaps the lower plate was obtained. Optimization of the upper plate overlap with respect to device area and radiation hardness was accomplished.

I. Introduction

Termination structures are employed by power semiconductor devices to increase their drain-source breakdown voltage to near the ideal, or parallel-plane value, which is set by the doping of the lightly-doped epitaxial region.[1] A cross-section of a typical integrated power DMOS device, showing two cells, is shown in figure 1. The termination region lies around the periphery of the cells.

In general, n-channel power-device breakdown voltage degrades with increasing radiation-induced positive trapped charge, N_{ot}.[2] Thus, a termination structure for power devices

in radiation environments must meet its breakdown specification for increasing values of N_{ot}. The two most frequently used termination methods are field plates (FPs) and field-limiting rings (FLRs). Although FLRs, when properly placed, can provide excellent radiation immunity,[2] they must be diffused very accurately for optimum performance.[3,4] FP termination structures, on the other hand, do not require such precise photolithographic control, and may even require less area than FLR designs for the same breakdown voltage in some cases. These and other processing considerations may make FPs an attractive alternative to FLRs.

The operation of an FP termination structure can be understood in terms of simple electrostatics. An FP induces charges in the semiconductor that effectively extend the junction they are terminating. In general, the more charges that an FP can induce in the semiconductor for a given voltage, the more effective the FP will be in raising the breakdown voltage. The charge induced by the FP is, of course, a strong function of oxide thickness under the FP. In n-channel devices, N_{ot} offsets some of the plate-induced charge, which translates directly into breakdown voltage degradation. In p-channel devices, N_{ot} enhances the plate-induced charge, which can lead to breakdown voltage enhancement.[5]

The maximum breakdown voltage for FP termination structures has been given as a function of oxide thickness for relatively low substrate doping.[6] However, in power-integrated circuit (PIC) devices, lower device voltage ratings are typical, which implies more heavily doped substrates. In this case, accurate prediction of the breakdown voltage can only be accomplished with two-dimensional simulation.
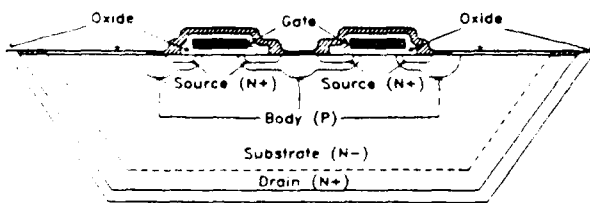

Figure 1. Representative cross-section of a power integrated DMOS device showing two cells.

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The breakdown voltage degradation of otherwise identical power DMOS devices with different two-level FP structures as a function of total ionizing dose was investigated. It was found that an upper field plate reduces the degradation somewhat. Also, an upper bound for the upper-plate overlap, beyond which no significant improvement in hardness results, was obtained. This distance defines the optimum upper-plate overlap, which is essential to minimizing device area.

II. Two-Dimensional Simulation

A. Method

Computer code designed to simulate the effects of ionizing radiation on the breakdown voltage of power semiconductor devices has been developed at the University of Arizona.[2] The code, entitled ASEPS (Arizona SEmiconductor Power device Simulator), solves Poisson's equation in two dimensions. Breakdown voltage is then determined by computing the ionization integral through the locus of highest-field points at every potential. ASEPS has proven to be an accurate and efficient simulator of highly reverse-biased junctions with arbitrary termination topologies and N_{ot}.[2] Its flexible input format enables comprehensive study of competing termination designs.

B. Parameters

The DMOS devices studied were all n-channel devices with a maximum achievable breakdown voltage of approximately 270 V (parallel-plane junction limit). All had a lower FP of fixed length (6.5 μm) and fixed oxide thickness (0.86 μm). The devices had upper-plate overlaps of either 0, 5, 10, or 15 μm and oxide thicknesses approximately three times
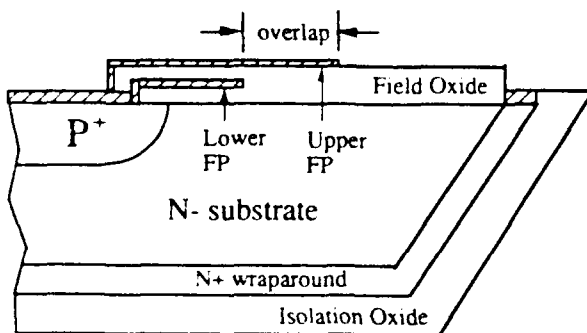

Figure 2. Cross section of the termination region of the devices in the text. A two-level FP termination structure is shown over the drain-body junction.

greater than the oxide under the lower plate. A qualitative cross-section of the termination region of these devices is shown in figure 2.

C. Modelling

ASEPS was used to gain insight into the effects of the upper field plate on breakdown voltage degradation. However, several considerations are necessary to obtain simulation results that accurately reflect experimental conditions. To do a completely accurate prediction of breakdown voltage degradation, ASEPS requires the equivalent charge at the Si-SiO$_2$ interface under the FP as a function of total iozing dose. This charge is taken to be constant with lateral position.

This mapping is difficult to obtain because, in general, reverse biasing the power device at, say, 100 V does not mean that the entire 100 V is dropped across the oxide under the FP, especially for low total dose. In fact, the electric field across the oxide under the FP depends on such things as substrate doping, oxide thickness under the FP, and N_{ot}. These variables are difficult to account for in a tractable test setup. Furthermore, since the electric field under the FP varies with lateral position, N_{ot} buildup under the field plate also varies with position. However, simulation can still be used to acquire insight into the breakdown performance of the devices under study.

To calibrate the simulations, simulation results were fit to experimental breakdown voltage versus total dose data for the device with 0 μm upper-plate overlap. Then the devices with 5, 10, and 15 μm overlap were simulated with the same values of N_{ot} as were used in the calibration. ASEPS output for three of these four devices are presented in figure 3. In these figures, the lines are equipotential lines, and the circles indicate highest electric-field points. A constant value of N_{ot} = 7 x 10^{11} cm^{-2} is assumed for all devices. This is the maximum equivalent value of N_c: ($N_{ot,max}$) under the FP, as explained in section III. It can be seen that the charges induced by the upper field plate in the semiconductor expand the equipotential lines, reducing the breakdown voltage degradation.

III. Experimental Results

The four device types (having different termination structures) were irradiated in a Co-60 source (dose rate approximately 20 $rad(Si)/min$) under constant reverse-bias voltage of 100 V to a total dose of nearly 150 $krad(Si)$. The

Worst-case experimental results are compared with simulation results in figure 4. The use of a hardened field oxide resulted in all devices tested having excellent resistance to breakdown degradation. In figure 4a, (worst-case) experimental breakdown voltage degradation, ΔBV, versus
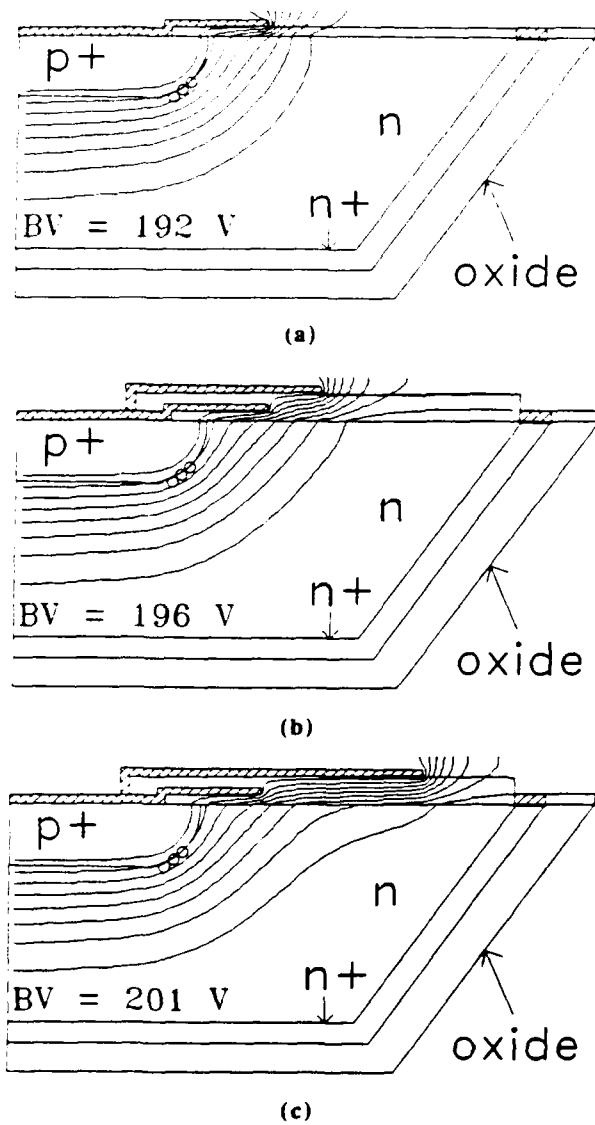

(a)

Figure 3. ASEPS simulation results showing the effect of increasing upper-plate overlap. $N_{ot} = N_{ot,sat} = 7.0 \times 10^{11}$ cm^{-2} is present in all devices. a) Lower plate only. b) 5 μm upper-plate overlap. c) 15 μm upper-plate overlap.
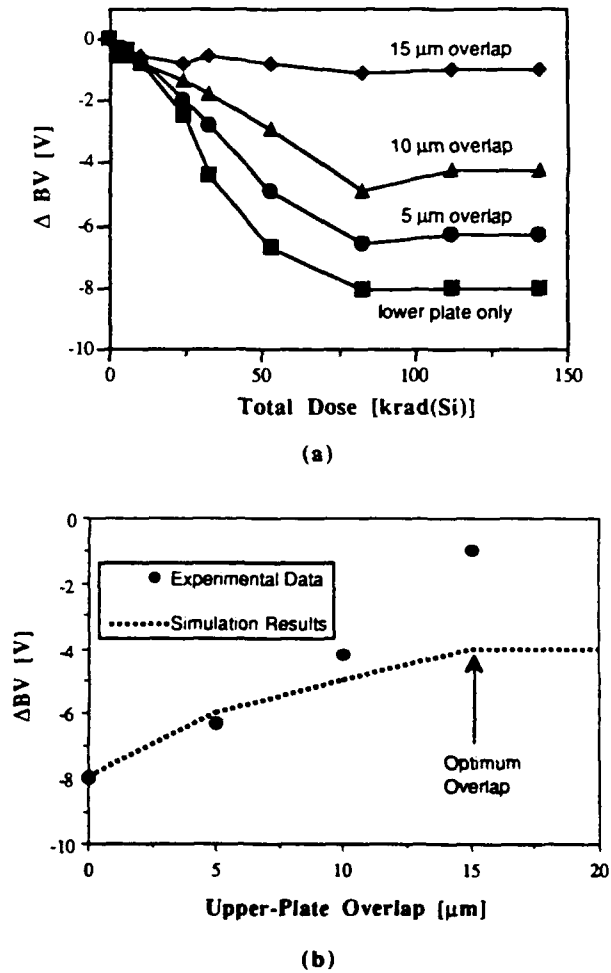

(a)

(b)

Figure 4. Comparison of ASEPS simulation results and experimental data. a) Experimental breakdown-voltage degradation as a function of total dose for the four devices discussed in the text. b) Change in breakdown voltage at 75 krad(Si) as a function of upper-plate overlap. The optimal overlap is identified as the overlap at which no improvement in hardness would result by increasing the overlap.

bias mimics the normal operating mode of the device in a typical circuit application. Breakdown voltage was taken to be the reverse-bias drain-source voltage that gave 1 mA of leakage current. The breakdown voltage of all devices, even the device with no upper FP, did not degrade beyond a total dose of 75 krad(Si); this implies that N_{ot} buildup saturated beyond 75 krad(Si).

plate length is shown. This data can be used to calibrate the ASEPS simulation results. If a linear relationship between total dose and N_{ot} is assumed for the range 0 - 75 krad(Si), a reasonable first-order model of N_{ot} buildup under the FP is obtained. N_{ot} is fixed, or saturated, at $N_{ot,sat}$ for all total doses beyond 75 krad(Si), in accordance with the experimental data.

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ΔBV is plotted versus upper plate overlap in figure 4b. The experimental data are taken for doses at or beyond 75 $krad(Si)$; accordingly, the simulation results assume $N_{ot} = N_{ot,sat} = 7.0 \times 10^{11} \, cm^{-2}$. In both figures, ΔBV, is plotted instead of absolute voltage so that chip-to-chip variations in initial breakdown voltage do not skew the comparison. All absolute voltages measured, however, were in the range 190 - 210 V, in agreement with simulation results. It can be seen that the optimum upper plate overlap is 15 μm, since further increases in upper-plate overlap would provide minimal additional hardness. If the degradation of the device with 0 μm upper-plate overlap can be tolerated, substantial savings in device area are possible.

IV. Conclusion

The breakdown-voltage degradation of an integrated-power DMOS device with several different termination structures was studied both experimentally and through two-dimensional simulation. It was shown that the presence of an upper field plate enhances the radiation hardness of the device, and that an optimal overlap can be predicted by simulation.

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IV.E Instructions for ASEPS

IV.E.1 Overview

ASEPS is a two-dimensional simulation program that has been tailored to the specific needs of power device breakdown voltage simulation. Specifically, the algorithms are tailored to handle large reverse-bias voltages and negligible current flow. In addition, ASEPS can handle arbitrary amounts of fixed charge at the Si-SiO$_2$ interface, which allows simulation of breakdown voltage in radiation environments. The simulations always converge independent of such parameters as grid spacing and biasing voltages. Typical simulation times on a 386-based machine with coprocessor are one minute for simple structures, and three minutes for more complex structures.

This description of ASEPS is written entirely from the user's point of view. That is, this description allows the user to begin simulating power device structures quickly.

To this end, several examples of typical structures are provided. They range from simple to more complex. By going through these examples, the user should be able to understand the basics of using ASEPS, and should be able to begin simulating new structures.

IV.E.2 Device Examples

EXAMPLE 1: MOS CAPACITOR

This simulation uses the following files, all of which should be in the INPUT directory: pmis.inp, pmis.txt, pmis1.imp

Since this is perhaps the simplest useful structure that one can imagine, it is worthwhile to look at these files individually to identify the features of ASEPS input files.

A. PMIS.INP

card1:   *device*   *qss=0.0E+12*   *fims=0.0*
This card specifies the amount of charge in cm-2 that is present at the Si-SiO2 interface, and the metal-semiconductor work function in Volts. It also has a variable "t" for temperature in degrees kelvin. The default is 300 K.

card2:   *geometry*   *scale=10.0*   *dwgfil = 'pmis.txt'*
This card specifies the scale of the drawing. In this case, scale = 10 because the

dimensions specified in the dwgfile, pmis.txt, should be multiplied by 10 to get the actual device dimensions.

card 3a: profile
card 3b: +   supfil(1)='pmis1.imp'
This card identifies the doping files used by the simulation. Since this structure has no pn junctions, it has only one doping file. In addition, the "+" symbol means continuation; if the specifications for one card take up more than one line, the "+" will extend the card to the next line.

card 4a: grid
card 4b   +   xstep=15   ystep=15   xslope=0.1   yslope=0.1
This card tells ASEPS how to construct it grids over the solution domain. Since this version of ASEPS can handle only 90 x 90 grid points, it may be necessary to adjust these values to ensure that the grid is sufficiently small. In general, decreasing xstep and ystep, or increasing xslope and yslope will cause the number of grid points to decrease. Changing these numbers does not substantially affect the accuracy of the results.

card 5:   material   mattyp(1)='Si'   mattyp(2)='SiO2'
This card identifies the material referenced in the pmisw.txt file. Several material types are possible; they are listed in the previous user's manual (attached).

card 6a: bias
card 6b: +   volt(1)=150.0   vsub=0.0
This card defines the bias on all of the conductors defined in the pmisw.txt file. Also, vsub is the voltage on the substrate, or on the bottom of the bulk.

card 7a: print   detail=.false.   printg=.false.   printc=.true.
card 7b: +   printv=.false.   printe=.false.   printm=.true.
card 7c: +   breakv=.true.   intface=.false.
This card contains all the options for printing information to the pmis.out file that is sent to the OUT directory. These are all covered in the previous document. The most important option is probably breakv, which tells ASEPS to compute the ionization integral. Also, we have found from experience that setting intface = .false. gives the most reliable results.

card 8a: plot   plotv=.true.   plote=.true.
card 8b: +   nlevel=9   nspot=5
This card contains the information ASEPS uses to create files for viewing with Auto-

CAD.

card 9: stop
This one is pretty self explanatory.

B. *PMIS.TXT*

The pmis.txt file appears below. Note that the spacing of the data is not flexible, although the order of the statements is flexible. All of the lines have the following format:

identifier   *x*   *y*   *dx*   *dy*   *code*

The identifier tells what type of region is being defined, and the x,y,dx,dy numbers define a rectangle whose lower left corner is at (x,y) and whose upper right corner is at (x+dx,y+dy). The code means different things for different identifiers.

In line 1, the "1" means that this conductor is biased at volt(1). In line 2, the "1" means that the impurity is diffused first. If there were a pn junction, there would be another IMPU line with a code of 2 or larger. In line 3, the "2" means that the material for the insulator is of mattype(2), or SiO_2. Finally, in line 4, the "1" means the material for the bulk, or the semiconductor substrate, is mattype(1), or Si.

line1:	*COND*	*0.000*	*1.600*	*1.500*	*0.100*	*1*
line2:	*IMPU*	*0.000*	*0.000*	*1.500*	*1.500*	*1*
line3:	*INSU*	*0.000*	*1.500*	*1.500*	*0.100*	*2*
line4:	*BULK*	*0.000*	*0.000*	*1.500*	*1.500*	*1*

As an added note, the previous manual suggests drawing the structure in AutoCAD initially and generating the <>.txt file through the export option. If you do this, you must go into the <>.txt file and make sure that all of the rectangles are touching each other without overlap and without gaps. Also, it is important to make sure that the lower left corner of the bulk starts at the origin. For these reasons, it is often easier to create the <>.txt file manually.

C. *PMIS1.IMP*

The following is the impurity file for this simulation. Some important facts to notice about this file are the following.

1. ASEPS ignores the first three lines of the file. So when you make your own doping files, it is not necessary to copy the "net", "depth", and "concen" information exactly,

or even at all. It is important, however, to make sure that you skip three lines before putting in any data.

2. Always start at 0.0. This is the surface concentration. The concentration can vary with depth, of course, although this example doesn't vary until the bottom of the structure (see 4).

3. The concentration is defined as (Donor Doping - Acceptor Doping). Thus, this is an MOS capacitor with a uniformly-doped p-type substrate (at $1e15$ cm^{-3}).

4. At the bottom of the structure, i.e. at 14 microns, the concentration begins to increase. This is to prevent the depletion region from punching through to the bottom of the structure. If this happens, ASEPS will not provide correct results, so it is always a good idea to include this in your doping file.

5. Doping files can specify dopings that are deeper than the boundaries for the bulk that are defined in the <>.txt file.

depth	net concen
0.000	-0.100E+16
1.000	-0.100E+16
2.000	-0.100E+16
4.000	-0.100E+16
6.000	-0.100E+16
8.000	-0.100E+16
10.000	-0.100E+16
11.000	-0.100E+16
12.000	-0.100E+16
13.000	-0.100E+16
14.000	-0.100E+17
15.000	-0.100E+18
16.000	-0.100E+18
17.000	-0.100E+18
18.000	-0.100E+18
19.000	-0.100E+18
20.000	-0.100E+20

D. SUMMARY

The above example illustrates the basic information needed to understand how the different input files relate to each other. If any of the information in these files is inconsistent with any of the others, ASEPS will not execute. It is important to check this should any errors occur.

EXAMPLE 2: PN JUNCTION

The next example is a pn junction. Only the features of the input files that are different from the MOS capacitor will be covered.

A. PN.INP

card1:   device   qss=0.0e+12   fims=0   t=300

card2:   geometry   dwgfil = 'pn.txt'   scale = 10.0

card3a: profile   supfil(1) = 'pn1.imp'
card3b: +   supfil(2) = 'pn2.imp'

Here, two impurity zones are specified. The first defines the background doping of the bulk, and the second defines the profile of the diffusion. The numerical order determines the order of diffusion as they would occur in a real device.

card4   grid   xstep = 10   ystep = 10   xslope = .1   yslope = .1

card5:   material   mattyp(1) = 'Si'   mattyp(2) = 'SiO2'

card6a: bias   volt(1) = 0.0
card6b: +   vsub = 185.0

The substrate is at a higher voltage than the diffusion. Thus, this is a p+ diffusion in an n+ substrate. Always make sure that the junction is not forward-biased. ASEPS will not recognize this; it will do the simulation, and give you an incorrect answer. Only reverse biased junctions are allowed.

card7a: print detail = .false.   printg = .false.   printc = .true.
card7b: +   printv = .false.   printe = .false.   printm = .true.
card7c: +   breakv = .true.   intface = .false.

card8a: plot   plotv = .true.   plote = .false.
card8b: +   nlevel = 8   nspot = 3

card9:   *stop*

B. PN.TXT

Here is the text file for this structure. The differences between this and the MOS capacitor
are
1. The COND is touching an IMPU zone; this is the biasing contact for the diffusion.
2. There are two IMPU lines, numbered to correspond with the definitions in PN.INP.
3. The IMPU diffusion that has code "2" extends for 10 microns; ASEPS will compute
    the lateral diffusion of the dopants using an aspect ratio of 0.8 and the junction depth.
    The junction depth is defined in PN2.IMP, to be covered later.

COND	*0.000*	*3.100*	*0.400*	*0.200*	*1*
IMPU	*0.000*	*0.000*	*3.600*	*3.100*	*1*
IMPU	*0.000*	*0.000*	*1.000*	*3.100*	*2*
INSU	*0.000*	*3.100*	*3.600*	*0.400*	*2*
BULK	*0.000*	*0.000*	*3.600*	*3.100*	*1*

C. PN1.IMP
This file looks similar to the doping file covered earlier for the MOS capacitor. Thus, it is
not included here.

D. PN2.IMP

This is the doping profile for the diffusion. There are a couple of things to notice.

1. This is really the file pn1.imp with the first few lines replaced by the p-type dopant
    concentration. It is a good idea to merely alter the doping file for the bulk when
    making doping files for diffusions.

2. The junction depth is 6.0 microns. At the junction depth, two concentrations must be
    specified. ASEPS will assign that point as the pn junction. If this is not done, ASEPS
    cannot find a junction, and will give incorrect answers.

	net
depth	*concen*
0.000	*-0.100E+19*
1.000	*-0.800E+18*
2.000	*-0.500E+18*

4.000	-0.600E+17
5.000	-0.100E+17
6.000	-0.100E+16
6.000	0.100E+16
8.000	0.100E+16
10.000	0.100E+16
11.000	0.100E+16
12.000	0.100E+16
13.000	0.100E+16
14.000	0.100E+16
18.000	0.100E+16
22.000	0.100E+16
23.000	0.100E+16
24.000	0.100E+16
25.000	0.100E+16
26.000	0.100E+16
27.000	0.100E+17
28.000	0.100E+18
29.000	0.100E+18
30.000	0.100E+20
31.000	0.100E+20
50.000	0.100E+20

EXAMPLE 3 FIELD PLATE

A commonly-used termination method for power devices is a field plate. This example uses the same doping files as the previous example.

A. FP.INP

```
device      qss=0.0e+12      fims=0      t=300

geometry    dwgfil = 'fp.txt'    scale = 10.0

profile     supfil(1) = 'fp1.imp'
+           supfil(2) = 'fp2.imp'

grid        xstep = 10     ystep = 10     xslope = .1          yslope = .1

material    mattyp(1) = 'Si'                mattyp(2) = 'SiO2'
```

bias   *volt(1) = 0.0*   *vsub = 205.0*

The applied voltage is higher because the structure probably has a higher breakdown voltage than the structure of example 2, which was an unterminated pn junction.

print	*detail = .true.*	*printg = .true.*	*printc = .true.*
+	*printv = .true.*	*printe = .true.*	*printm = .true.*
+	*breakv = .true.*		

plot	*plotv = .true.*	*plote = .false.*
+	*nlevel = 8*	*nspot = 3*

stop

B. FP.TXT

Compared to PN.TXT, there is one extra COND line, but with the same bias code as the junction biasing voltage. This is the field plate. Note that it overlaps the junction contact, and that it extends approximately 12 μm from the edge of the pn junction. The junction extends 10 + (0.8)(6.4) = 15.12 μm from the left edge of the structure, and the field plate is 10 + 17 = 27 μm from the left edge. The difference is the length of the field plate. Finally the oxide thickness under the field plate is 1.9 μm.

COND	0.000	3.100	0.400	0.200	1
COND	1.000	3.290	1.700	0.100	1
IMPU	0.000	0.000	3.600	3.100	1
IMPU	0.000	0.000	1.000	3.100	2
INSU	0.000	3.100	3.600	0.400	2
BULK	0.000	0.000	3.600	3.100	1

C. FP1.IMP and FP2.IMP

These are identical to PN1.IMP and PN2.IMP

EXAMPLE 4: FIELD LIMITING RING

The last example is a field-limiting ring termination structure. Again, only the features of this simulation that differ from the previous examples will be pointed out. Since this version of ASEPS can only handle 90 by 90 grid points, only one or two rings can be simulated. A multi-ring example is a straightforward extension of the single-ring example.

A. 1R.INP

```
device         qss=0.0e+11      fims=0     t=300


geometry       dwgfil = '1r.txt'            scale = 10.0


profile        supfil(1) = '1r1.imp'
+              supfil'^' = '1r2.imp'
```
This is the diffusion for the main junction
```
+              supfil(3) = '1r3.imp'
```
This is the diffusion for the field-limiting ring

```
grid           xstep = 5     ystep = 5     xslope = 0.1     yslope = 0.1


material       mattyp(1) = 'Si'             mattyp(2) = 'SiO2'


bias           volt(1) = 0.0
```
This is the bias on the main junction
```
+              volt(2) = 140.0
```
This is the bias on the field-limiting ring. It is calculated by the method given by Kang-Deog Suh, Soon-Won Hong, Kwyro Lee, and Choong-Ki Kim, "An Analysis for the Potential of Floating Guard Rings," *Solid-State Electronics*, vol. 33, No. 9, pp. 1125-1129, 1990.

```
+              vsub = 240.0
```
This is the bias across the entire device (drain bias). Note that the breakdown voltage of this structure is higher than the field-plate structure.

```
print          detail = .false.     printg = .true.     printc = .false.
+              printv = .false.     printe = .false.     printm = .true.
+              breakv = .true.      intface = .false.


plot           plotv = .true.       plote = .false.
+              nlevel = 8           nspot = 5


stop
```

B. 1R.TXT

COND	*0.000*	*3.100*	*0.400*	*0.200*	*1*

main junction conductor; its lower edge must be at the oxide- silicon interface

COND	*2.900*	*3.100*	*0.400*	*0.256000*	*2*

field-limiting ring conductor.

IMPU	*0.000*	*0.000*	*7.000*	*3.100*	*1*

background (epi-layer) doping

IMPU	*0.000*	*0.000*	*1.300*	*3.100*	*2*

main junction diffusion

IMPU	*2.900*	*0.000*	*0.400*	*3.100*	*3*

field-limiting ring diffusion

INSU	*0.000*	*3.100*	*7.000*	*0.400*	*2*
BULK	*0.000*	*0.000*	*7.000*	*3.100*	*1*

1R1.IMP, 1R2.IMP, and 1R3.IMP are the same as has been covered previously.

IV.E.3   Conclusion

This information should allow a user to get started simulating simple structures in ASEPS quickly. There are other features of ASEPS that have not been covered here. For these, the reader is referred to the previous user's manual. All of the examples described here should be included in the INPUT directory supplied with the program. The user is encouraged to run these examples before attempting to simulate more involved structures.

V.   Charge Buildup in Field Oxides

V.A   Introduction

The basic problem addressed in this project was correlating the radiation-induced charge to the total dose in power-device termination structures. This work is the result of a review of the UA program (participants included Cohn, Galloway, Schrimpf, Platteter, Titus, Dawes) held at Kaman-Tempo on 8 February 1990. The work done on this project "solves" the problem that was posed at that meeting. The details of the solution are discussed in a paper that was presented at the 1991 IEEE Nuclear and Space Radiation Effects Conference. The paper is summarized here and the text is included in Section V.B.

Section V.B.: S.L. Kosier, R.D. Schrimpf, K.F. Galloway, and F.E. Cellier, "Predicting Worst-Case Charge Buildup in Power-Device Field Oxides," *IEEE Trans. Nucl. Sci.*, vol. NS-38, pp. 1383-1390, 1991.

This paper makes the link, for the first time, between charge buildup in field oxides of test structures (such as MOS capacitors and lateral MOSFETs) and charge buildup in field oxides of power devices. This information is critical for designing radiation-tolerant power devices. Previous work has focused on minimizing sensitivity to oxide charge with no regard as to how much charge can realistically be expected in the structure. This work provides a closed-form worst-case expression for how much charge will accumulate in the power device field oxide. This expression is suitable for design purposes.

Previously, continuous and uniform buildup of oxide charge with total ionizing dose was assumed to occur in every termination structure. This work allows prediction of the charge-saturation effects that are seen in actual device structures. Devices can now be designed to accumulate only as much charge as desired. Previously, charge buildup was modeled as being uniform with lateral position; here, the reality of nonuniform charge buildup is shown and a method to simulate it is provided. The models rely on the field-collapse model of charge buildup in the oxide; however, the methods described in the paper will work for any other relationship between charge buildup and electric field in the oxide. The methods and procedures are simple and predictive. They can be applied immediately to radiation-hardened power device designs.

ASEPS played an important role in establishing the link between experimental breakdown-voltage degradation data and charge buildup in the field oxide. The devices tested in the work were DMOS devices developed at AT&T Bell Labs as part of the Rad-Hard PIC Development program.

V.B Predicting Worst-Case Charge Buildup in Power Device Field Oxides

PREDICTING WORST-CASE CHARGE BUILDUP IN POWER-DEVICE FIELD OXIDES[†]

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ABSTRACT

Existing models for worst-case charge buildup in silicon dioxide are applied to single- and two-level field plate termination structures in n-channel power MOSFETs. It is shown that the field-collapse model, when properly applied to these termination structures, provides excellent agreement between experimental and simulation worst-case breakdown-voltage degradation results. Nonuniform charge buildup in the termination structure field oxide is identified, and two methods of doing device simulation that take the nonuniformity into account are introduced. Finally, simple analytical models are presented that enable the nonuniform charge distribution to be calculated for any field-plate structure.

Figure 1. Representative cross section of an n-channel VDMOS power device.

I. INTRODUCTION

In a vertical power DMOS (VDMOS) device, shown schematically in figure 1, the individual MOS cells are surrounded by the termination structure. The MOS Region defines the current handling capability of the device, while the Termination Region sets the breakdown voltage of the device [1]. Termination structures are built in the termination region to raise the breakdown voltage of the drain-body junction to near its ideal value. Field Plate (FP) termination structures are common in VDMOS devices, especially low-voltage, integrated devices, due to their small area consumption and relative processing ease [2]. FP structures, used in conjunction with highly-resistive Semi-Insulating Polycrystalline Silicon (SIPOS) films, are also found in high-voltage (1 kV or more) devices [3 – 6]. Finally, all integrated power devices have a "parasitic" FP in the form of the source contact [7]. Thus, the basic FP structure, and its response to ionizing radiation, is of great interest to power-device designers.

The field oxide (FOX) under the FP will collect charge in radiation environments, so the charge must be accounted for in the rad-hard power-device design process. Net positive oxide-trapped charge at the oxide-silicon interface, N_{ot},

degrades the breakdown voltage, BV, of n-channel power devices [8 – 10], and may degrade the breakdown voltage of p-channel power devices [11]. For power-device design purposes, only the worst-case value of N_{ot}, $N_{ot,wc}$, is of interest, since it is this value that must be considered when the voltage rating of the device is specified.

This work introduces a technique for obtaining the $N_{ot,wc}$ distribution in a FP FOX, as well as methods to account for this distribution in device simulation. The methods are verified by comparing experimental breakdown-voltage degradation data with two-dimensional simulation results. Simple analytical equations are derived that enable prediction of the $N_{ot,wc}$ distribution in any FP FOX solely in terms of device parameters and applied voltage. The methods are simple and predictive, and can be used to gain insight into the charge buildup process in the FP FOX.

The device simulator used in this work was *Arizona Semiconductor Power Device Simulator* (ASEPS) [8, 12]. ASEPS solves Poisson's equation in two dimensions and determines breakdown voltage by computing the ionization integral. ASEPS' numerical algorithms are specifically tailored for solving highly reverse-biased junctions; its rapid execution speed, guaranteed convergence, and flexible input format make it a powerful tool for power-device simulation and design.

II. Experiment

A. Method

To predict worst-case charge buildup in the FP FOX, the radiation response of the FOX under the bias polarity present during normal operation of the power device must be determined. Lateral p-channel transistors with FOX as the gate dielectric, shown in figure 2a, were used for this purpose. Relevant device parameters of the n-channel power DMOS transistors with FP are shown in figure 2b. Only the termination region is shown, since it alone determines the BV of the device. The pre-irradiation BV of all the DMOS devices was approximately 200 V.

The FOX in both devices in figure 2 comes from the same process; the thickness difference between the two device types was a result of longer growth time for the FOX in figure 2a. Note that the thickness difference is not crucial, since the role of the device in figure 2a is only to identify the appropriate model for worst-case charge buildup in the FOX.

Several samples of both devices were concurrently irradiated in a Co-60 source (dose rate approximately 20 $rad(Si)/min$). During irradiation, both device types were biased at a constant voltage, V_{tot}, of either 0 V or 100 V. Charge buildup in the FOX transistors and breakdown voltage of the DMOS devices was measured at several values of total ionizing dose, D. Charge buildup was measured in the p-channel FOX devices using the mid-gap method [13], and BV of the DMOS devices was defined as V_{DS} when $I_{DS} = 1$ mA.

B. Results

The experimental N_{ot} and breakdown voltage degradation, ΔBV, vs. D curves are shown in figure 3a and 3b, respectively. Negligible N_{it} formation was observed in the p-channel FOX devices, indicating negligible N_{it} formation in the FP FOX as well.

As shown in figure 3a, saturation of N_{ot} buildup in the device of figure 2a is bounded by the prediction of the field-collapse (FC) model for negatively-biased oxides [14]. The FC model asserts that N_{ot} buildup saturates when the trapped charge in the oxide compensates the charge on the gate electrode. The electric field in the oxide goes to zero, and subsequent electron-hole pairs, ehps, efficiently recombine, leading to negligible additional charge buildup. Under this assumption, $N_{ot,wc}$ is [14]
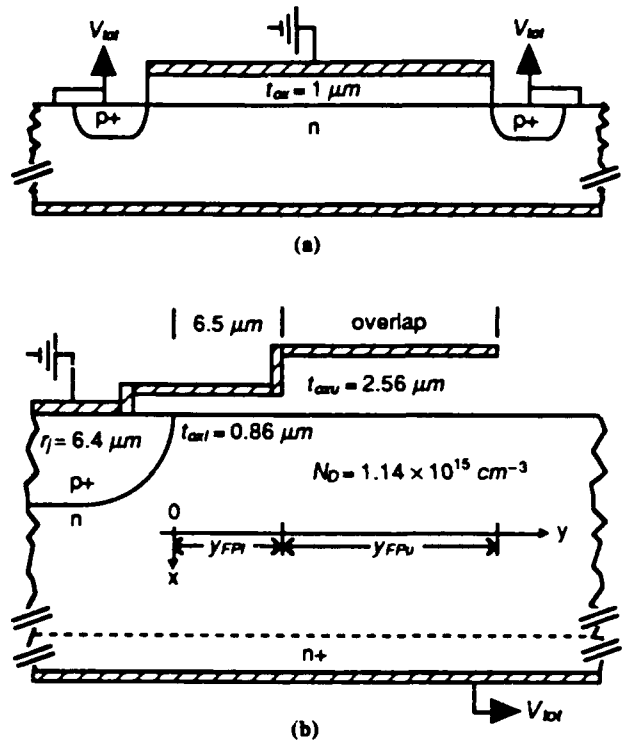
Figure 2. Schematic cross-sections of devices described in text. (a) P-channel lateral FOX transistor. (b) Termination region of n-channel DMOS transistors with FP termination structures.

$$N_{ot,wc} = \frac{C_{ox}|V_{ox}|}{q} \tag{1}$$

where V_{ox} is the voltage across the oxide, C_{ox} is the oxide capacitance per unit area, and q is the magnitude of the electronic charge. In the device of figure 2a, the negatively-biased gate forms an inversion layer in the silicon, so most of the applied voltage is dropped across the FOX. That is, $V_{ox} = V_{tot}$, and equation (1) gives $N_{ot,wc} = 2.16 \times 10^{12}$ cm^{-2}, which is indicated at the top of figure 3a. Note also that when $V_{tot} = 0$ V, equation (1) predicts that $N_{ot,wc} = 0$ cm^{-2}, which, although clearly an approximation, is consistent with the bottom curve of figure 3a. In fact, the metal-silicon work-function difference, if taken to be on the order of a 1 V, gives $N_{ot,wc} = 2.15 \times 10^{10}$ cm^{-2}, which is a more realistic value. Thus, the FC model, as expressed in equation (1), adequately predicts $N_{ot,wc}$ for the device of figure 2a.

As indicated in figure 3b, ΔBV, and thus N_{ot} buildup under the FP, saturates for $D > 75$ $krad(Si)$ for the DMOS devices biased at $V_{tot} = -100$ V. The devices with $V_{tot} = 0$ V had
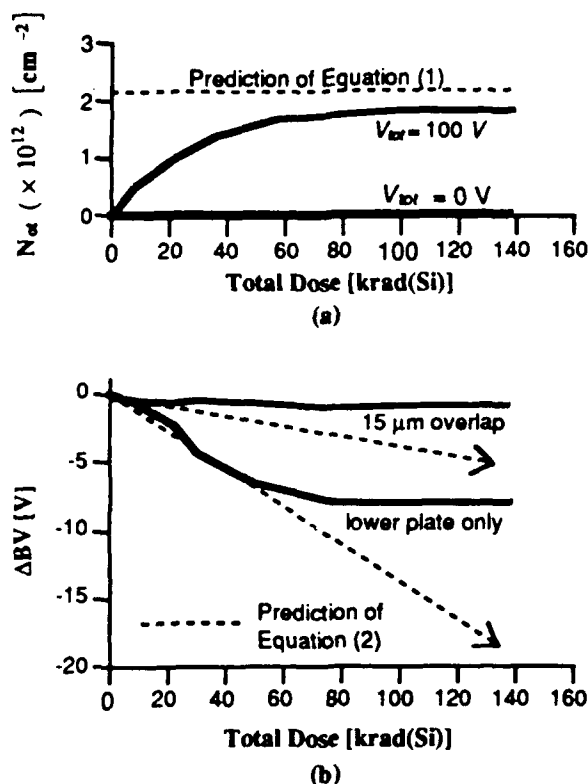
where G is the generation rate of *ehps* per unit volume and F is the equivalent fraction of holes trapped at the oxide-silicon interface. For worst-case calculations at low total doses, it has been assumed that $F = 1.0$ [15]. In later work [8, 10], F has been determined by fitting equation (2) to experimental data.

It is seen immediately that equation (2) is of limited utility for estimating worst-case N_{ot} buildup in the FP FOX. That is, although an appropriate value for F can be found for the devices biased at $V_{tot} = 0$ V, $(F = 0)$, an appropriate value for F cannot be found for the biased devices because, as mentioned previously, ΔBV, and thus N_{ot} buildup, saturates for $D > 75$ *krad(Si)*. Equation (2) can only be applied if it is recognized that F is a function of electric field in the oxide, which, in turn, is a function of N_{ot} already in the oxide. This analysis must be performed iteratively by computer. The result of such an analysis for the bias condition depicted in figure 2 is essentially equation (1) [14].

The assumption implicit in equation (2) is that N_{ot} buildup is uniform across the entire structure. This is a gross approximation, as will be shown in the next section.

B. Application of the Field-Collapse Model to the FP FOX

Since the FC model adequately predicted $N_{ot,wc}$ for the devices of figure 2a, it seems likely that the FC model, when properly applied, can predict $N_{ot,wc}$ in the FP FOX, and thus predict $\Delta BV(max)$ for the devices of figure 2b. If equation (1) is blindly used for this purpose (that is, let $t_{ox} = 0.86$ μm and $V_{ox} = V_{tot}$ in equation (1)), $N_{ot,wc} = 2.5 \times 10^{12}$ cm^{-2}. If this value of N_{ot} is then used in an ASEPS simulation of the device of figure 2b, ΔBV is very large for all devices, regardless of overlap (greater than 30 V). However, experimental $\Delta BV(max)$ of the DMOS device with lower plate only was 8 V, and $\Delta BV(max)$ of the device with 15 μm overlap was 1.5 V. Devices with 5 and 10 μm overlaps had experimental $\Delta BV(max)$ of 6 and 4 V, respectively. Clearly, naive application of equation (1) overestimates $N_{ot,wc}$ in the DMOS FOX.

The reason equation (2) can be used directly to predict $N_{ot,wc}$ for the structure of figure 2a is that $V_{ox} = V_{tot}$. However, $V_{ox} < V_{tot}$ in an FP structure due to the large voltage drop in the depletion layer under the FP, which is supported by the adjacent p^+-n junction. Furthermore, V_{ox} varies with lateral position, y. These facts explain why naive application of the FC model to the FP FOX was unsuccessful. A more sophisticated application of the FC model is needed. This requires that the operation of the FP termination structure be

Figure 3. Comparison of experimental data (heavy lines) and predicted response (dashed lines). (a) N_{ot} vs. D for device of figure 2a. (b) ΔBV vs. D for devices of figure 2b.

$\Delta BV = 0$ V for all values of D; this data is not shown in figure 3b or in subsequent figures. The ΔBV vs. D results are qualitatively consistent with the predictions of the FC model. Applying the FC model as expressed in equation (1) directly to the DMOS device is not appropriate, however, since it would greatly overestimate the maximum breakdown-voltage degradation of the structure, $\Delta BV(max)$. This issue, along with a brief review of previous work in modeling charge buildup in power-device termination structures, is addressed in the next section.

III. CHARGE BUILDUP IN THE DMOS FOX

A. Previous Work

Earlier modeling of breakdown voltage degradation of power MOSFETs [8, 10] has assumed that N_{ot} in the termination structure FOX increases linearly with D via

$$N_{ot} = D \, t_{ox} \, G \, F \, , \qquad (2)$$

examined to uncover the physical mechanisms that lead to breakdown-voltage degradation in ionizing-radiation environments.

The means by which the FP raises the BV of the device, and the reason N_{α} degrades BV, can be interpreted with charge-balancing arguments. Note that under normal n-channel DMOS bias conditions, the x-component of the electric field in the FOX is negative. Electric field lines originate on positive ionized donors in the depletion layer under the FP and terminate on either negative charge on the FP or on ionized acceptors in the p$^+$ body. It is the termination of depletion-layer charge on the FP that gives rise to the finite E_x in the oxide; the finite E_x also raises the BV of the junction.

Under these bias conditions, ionizing-radiation-induced holes will drift toward the FP and possibly be trapped near the oxide-metal interface, where they compensate negative charge on the FP. As more positive charge accumulates, fewer positive ions will be uncovered in the depletion layer, and as a result the BV of the device degrades.

The FC model holds that charge buildup will continue in the DMOS FOX until E_x goes to zero at every point in the oxide. This can only happen when the trapped hole distribution in the oxide compensates charge on the FP such that the "effective" voltage on the FP seen from the semiconductor is the same as the surface potential of the unterminated junction. That is, the trapped holes must entirely negate any effect of the FP, as seen from the semiconductor, in order to force E_x to zero at every position y in the FOX. In terms of measurable quantities, the trapped hole distribution forces the pre-irradiation surface potential under the FP, $\psi_{s,FP}(y)$ to be the same as the surface potential of the unterminated p$^+$-n junction, $\psi_{s,pn}(y)$. The charge required to bring about this shift in $\psi_s(y)$ is seen to be directly proportional to the change in $\psi_s(y)$. $N_{\alpha,wc}(y)$ can be obtained, then, by finding $\psi_{s,FP}(y)$, subtracting it from $\psi_{s,pn}(y)$, and using this difference in equation (1). Explicitly,

$$N_{ot,wc}(y) = \frac{C_{ox}\left(\psi_{s,pn}(y) - \psi_{s,FP}(y)\right)}{q} \qquad (3)$$

can be used to approximate $N_{\alpha,wc}(y)$ in the FP FOX. The only approximation in equation (3) is using C_{ox}; the appropriate capacitance for the voltage difference is actually the series combination of C_{ox} and depletion-layer capacitance, C_{dep}. Since this combination, if it were taken into account, would only underestimate $N_{\alpha,wc}(y)$, the approximation does not affect the worst-case nature of the method.

C. Results

The structure with 15 μm overlap will be used to illustrate the methods outlined in the previous section. To demonstrate the generality of the methods, they will also be applied to the structure with lower plate only. In the graphs that follow, data points are simulation results, while dashed lines are analytical model predictions. The model is covered in the Appendix.

Figure 4 shows $\psi_{s,FP}(y)$ and $\psi_{s,pn}(y)$ of the structure with 15 μm overlap. A schematic of the two-level FP structure is provided for reference. Figure 5 shows $N_{\alpha,wc}(y)$ as defined by equation (3), using $\psi_{s,FP}(y)$ and $\psi_{s,pn}(y)$ from figure 4.
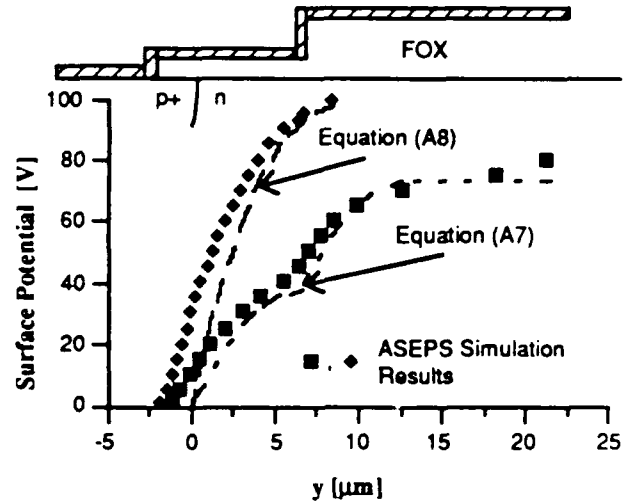
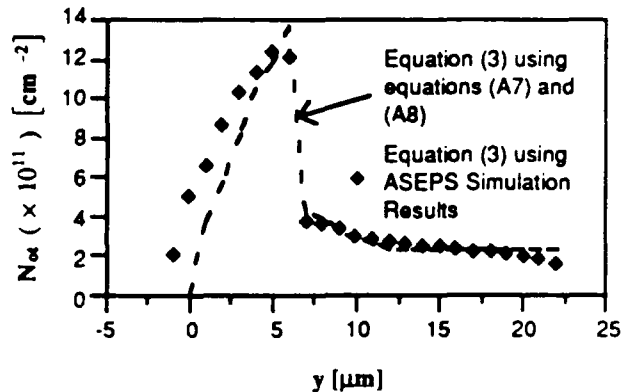**Figure 4.** Surface potential under the two-level FP and of the unterminated junction.

Figure 5. $N_{ot,wc}$ under the two-level FP.

The $N_{\alpha,wc}(y)$ profile under the two-level FP is highly nonuniform, and attains its maximum value, $N_{\alpha,wc}(max)$ near the edge of the lower FP. $N_{\alpha,wc}(max)$ is approximately

1.3×10^{12} cm^{-2}, which is far less than the $\therefore \, 5 \times 10^{12}$ cm^{-2} predicted by naive application of the FC model.

D. Accounting for Nonuniform N_{ot} in Device Simulation

All currently-available device simulators do not handle nonuniform N_{ot} distributions. However, the effect of the $N_{ot,wc}(y)$ profile on $\psi_s(y)$, and thus on $\Delta BV(max)$, can be reproduced without this capability.

One way to account for the $N_{ot,wc}(y)$ distribution is to find its average value under the FP, $\overline{N_{ot,wc}}$, given by

$$\overline{N_{ot,wc}} = \frac{1}{y_{FPl} + y_{FPu}} \int_0^{y_{FPl} + y_{FPu}} N_{ot,wc}(y) \, dy \quad (4)$$

and perform the simulation with uniformly-distributed N_{ot} equal to $\overline{N_{ot,wc}}$. Using the $N_{ot,wc}(y)$ data in figure 5, $\overline{N_{ot,wc}}$ = 5.1×10^{11} cm^{-2}. ASEPS simulations with uniformly-distributed N_{ot} equal to $\overline{N_{ot,wc}}$ gives $\Delta BV(max) = 4$ V.

If still more accurate simulation results are desired, the $N_{ot,wc}(y)$ distribution in figure 5 must be taken into account explicitly. That is, instead of modeling the trapped holes by N_{ot} at the oxide-silicon interface, the same effect can be achieved by altering the potential on the FP to reflect the presence of the trapped holes at the oxide-metal interface. This is done by segmenting the FP into many segments, and assigning each segment a different bias, $V_{FP,i}$, given by

$$V_{FP,i} = \overline{\psi_{s,pn}(y)}_i - \overline{\psi_{s,FP}(y)}_i . \quad (5)$$

In equation (5), i = 1...# of segments and $\overline{\psi_{s,pn}(y)}_i$ and $\overline{\psi_{s,FP}(y)}_i$ denote the average value of $\psi_{s,pn}(y)$ and $\psi_{s,FP}(y)$ through the ith segment. The concept is illustrated schematically in figure 6.

ASEPS simulations with segmented FP biased at $V_{FP,i}$ give $\Delta BV = 3$ V. ASEPS simulation output, both before irradiation and with segmented FP, is shown in figure 7. The lines are equipotential lines and circles indicate highest-field points.

Figure 8 presents ASEPS estimates of $\Delta BV(max)$ for the structure with 15 μm overlap obtained three different ways. Line (A) was obtained by segmenting the FP and biasing each segment separately, as shown schematically in figure 6; line (B) was obtained by assuming uniformly-distibuted N_{ot} equal to $\overline{N_{ot,wc}}$; and line (C) was obtained by assuming
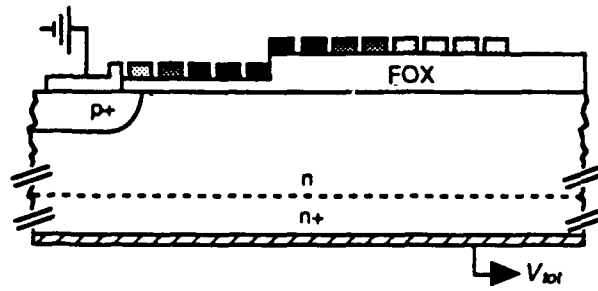
Figure 6. Schematic illustration of segmented FP for device simulation. Darker segments have larger V_{FP} applied to them.
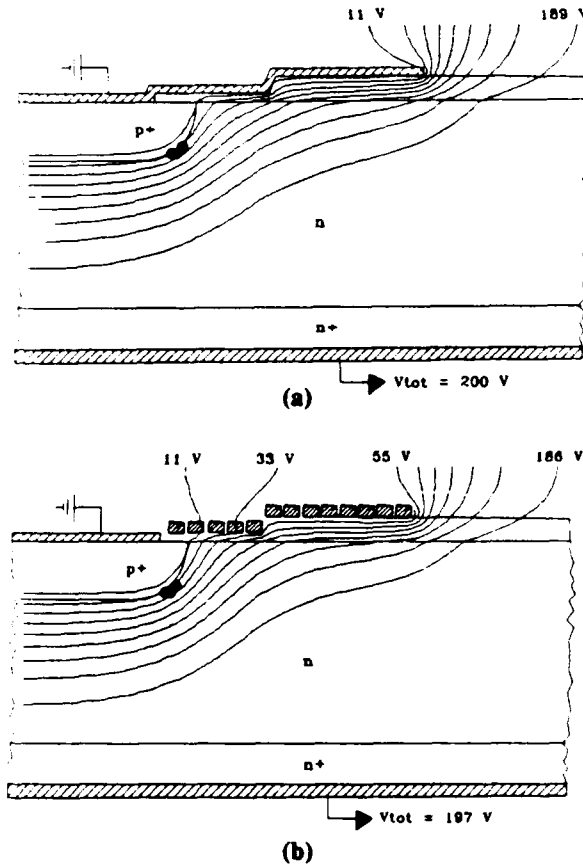
Figure 7. ASEPS simulation output. (a) Two-level FP with $BV = 200$ V, $N_{ot} = 0$ cm^{-2}. (b) Segmented two-level FP as in figure 6. $BV = 197$ V.

uniformly-distributed N_{ot} equal to $N_{ot,wc}(max)$. Clearly, agreement between simulation and experiment is improved by accounting for the $N_{ot,wc}(y)$ distribution when doing device simulations. Figure 9 presents the same information as figure 8 for the structure with lower plate only, illustrating the generality of the methods outlined above.
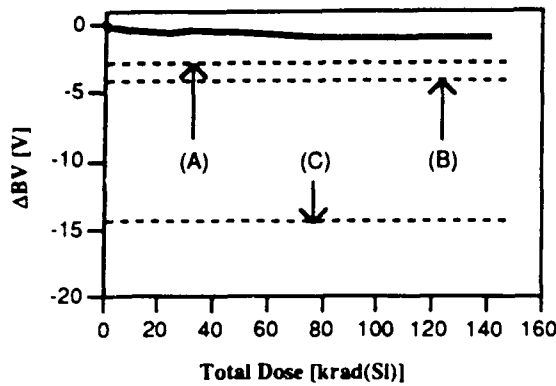
Figure 8. ΔBV vs. D for the DMOS device with 15 μm overlap. The heavy line is experimental data. (A), (B), and (C) represent ASEPS estimates of $\Delta BV(max)$ as described in the text.
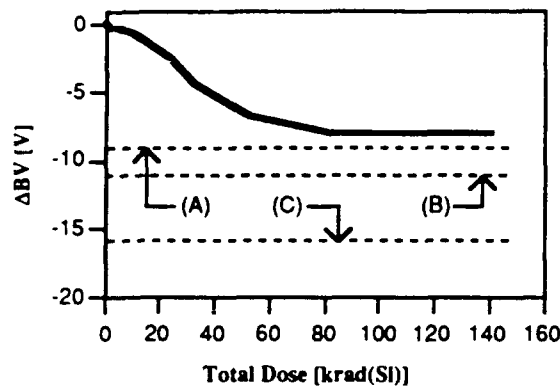

Figure 9. ΔBV vs. D for the device with lower plate only. The heavy line is experimental data. (A), (B), and (C) represent ASEPS estimates of $\Delta BV(max)$ as described in the text.

It is seen that by accounting for the nonuniform charge buildup, simulation results of $\Delta BV(max)$ closely approximate experimental data. The segmented FP gives more accurate estimates of $\Delta BV(max)$ than does equation (3), but it is also somewhat more cumbersome. Note, however, that the segmented FP method employs no approximations whatsoever, beyond discretizing the continuous $\psi_{s,pn}(y)$ and $\psi_{s,FP}(y)$ distributions. If nonuniform N_a were somehow incorporated into the simulation, the $N_{ot,wc}(y)$ distribution would necessarily be approximate due to the uncertainties in the correct value of capacitance at every point under the FP, as discussed at the end of section III.B.

The utility of precise knowledge of the $N_{ot,wc}(y)$ distribution in the DMOS FOX for device simulation has been

established. Simple equations for determining $\psi_{s,FP}(y)$ and $\psi_{s,pn}(y)$, which can be used directly in equation (4) to obtain $N_{ot,wc}(y)$, are presented in the Appendix.

IV. SUMMARY

Existing models for charge buildup in silicon dioxide were applied to power-device field oxides with the purpose of estimating worst-case charge buildup. Proper application of the field-collapse model allowed an estimate of the $N_{ot,wc}(y)$ distribution in the FP FOX to be generated. Two methods of taking this distribution into account for device simulation were introduced. Agreement between experimental and simulation $\Delta BV(max)$ was excellent, validating the method of obtaining $N_{ot,wc}(y)$. Simple equations are presented that allow the $N_{ot,wc}(y)$ distribution to be generated for any FP structure in terms of device parameters and applied voltage.

APPENDIX

The first step in obtaining $\psi_{s,FP}(y)$ is to find the maximum voltage across the oxide, $V_{ox}(max)$. $V_{ox}(max)$ is entirely determined by the characteristics of the depleted MOS capacitor that exists under the FP far from the drain-body junction. $V_{ox}(max)$ can be found in closed form by solving for the maximum value of the surface potential, $\psi_{s,FP}(max)$, and noting that $V_{ox}(max) = V_{tot} - \psi_{s,FP}(max)$.

Far from both the drain-body junction and the edge of the FP, and with negligible N_{ot} in the FOX, Gauss' law at the oxide-silicon interface is

$$\kappa_{ox} E_{ox} = \kappa_{Si} E_{Si}, \tag{A1}$$

where E_{ox} and E_{Si} are the x-components of the electric field in the oxide and silicon, and κ_{ox} and κ_{Si} are the relative permittivities of silicon dioxide and silicon, respectively. Using the depletion approximation in the x-direction, $\psi_{s,FP}(max)$ can be written as

$$\psi_{s,FP}(max) = \frac{\kappa_{Si} \, \epsilon_o E_{Si}(max)^2}{2 q N_D}, \tag{A2}$$

where $E_{Si}(max)$ is the maximum value of E_{Si}, N_D is the doping of epitaxial drain, and ϵ_o is the permittivity of free space. Solving equation (A1) for E_{Si}, and noting that $E_{ox}(max) = V_{ox}(max)/t_{ox}$, it follows that $E_{Si}(max)$ is

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ACKNOWLEDGMENTS

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VI. 1/f Noise in Power MOSFETs

VI.A Introduction

A thorough understanding of the nature of radiation-induced charge in power MOSFETs is required to determine the suitability of particular device types for applications in radiation environments. Measurements of the spatial and energy densities of interface and oxide trapped charge are essential to this work. Several techniques currently exist for characterizing these charge densities, including subthreshold-slope measurements, charge pumping, and capacitance-voltage measurements. Each of these techniques is useful, but each also has shortcomings, particularly when applied to power MOSFETs. This project examined the use of 1/f noise measurements for characterizing radiation-induced interface traps and oxide trapped charge in power MOSFETs. The term "1/f noise" is used generically to refer to all noise that is described by an equation of the form:

$$S(f) = \frac{A}{f^{\lambda}} \tag{1}$$

where f is the frequency, $S(f)$ is the noise spectrum, and A and λ are constants.

The 1/f noise behavior of MOSFETs has been studied extensively in recent years. It has been reported by various authors that a relationship exists between the density of traps near the Si/SiO$_2$ interface and the 1/f noise present in the device. Several detailed models for 1/f noise in MOSFETs have been presented, but there is still disagreement over the validity of each. These models are usually classified as number-fluctuation models, mobility-fluctuation models, or combinations of the two. 1/f noise measurements currently are not widely used to measure the density of interface traps in MOS transistors that have been exposed to ionizing radiation. A correlation between preirradiation 1/f noise and radiation hardness has been observed in integrated MOSFETs, but the physical reasons for the correlation have not been established.

There are currently several other methods in use for obtaining information on radiation-induced interface states. The stretchout of capacitance-voltage curves can be used, but this method requires the use of MOS capacitors rather than transistors. This may not be possible in some cases, and the capacitor characteristics may be different than those of actual devices.

Measurements can be made directly on MOSFETs by using subthreshold-slope or charge-pumping techniques. The slope of the $\ln(I_D)$-V_G characteristic of a MOSFET

operating between flatband and threshold is sensitive to the density of interface states. A commonly-used method separates the effects of interface traps and trapped-oxide charge using the radiation-induced change in the subthreshold characteristics. However, power-MOSFET post-radiation subthreshold characteristics may not be described well by straight lines on a semi-log plot. This makes it difficult to define a single slope, and may affect the accuracy adversely.

Charge-pumping measurements have been shown to be a convenient and reliable means of obtaining the density of interface states in MOS transistors. In this technique, the source and drain junctions are reverse biased and the gate is pulsed between inversion and accumulation. The substrate current under these conditions is proportional to the density of interface states. In power MOSFETs, however, the substrate is not electrically accessible and charge pumping is not possible.

While subthreshold measurements and charge pumping are both useful techniques, they both have limitations when applied to power MOSFETs. This work examined the use of $1/f$ noise measurements as a tool for measuring radiation-induced charge in power MOSFETs.

N-channel and P-channel MOSFETs were exposed to ionizing radiation in a Co-60 source. The interface-trap density was compared to the noise spectrum at each measurement point to establish the relationships among noise voltage, bias conditions, and interface-trap density. In addition the relationship between pre-irradiation noise and charge buildup was examined. The devices were characterized using the subthreshold-slope technique in addition to $1/f$ noise measurements to allow comparison between the noise properties and the radiation-induced charge densities.

Noise measurements were made using a system consisting of a low-noise preamplifier and a Hewlett-Packard 3582A spectrum analyzer. The test system allows devices to be biased in either the linear or saturation region.

The papers describing the work on $1/f$ noise are included in Sections VI.B and VI.C. A brief overview of each paper is included here to guide the reader through this material.

Section VI.B: J.A. Babcock, J.L. Titus, R.D. Schrimpf, and K.F. Galloway, "Effects of Ionizing Radiation on the Noise Properties of DMOS Power Transistors," *IEEE Trans. Nucl. Sci.*, vol. NS-38, pp. 1304-1309, 1991.

This paper describes the variation of both A and λ from Eq. (1) with total dose. The devices are operated in the saturation region. No correlation is found between pre-rad noise and radiation hardness

This paper shows that measurements of power-MOSFET 1/*f* noise made in the linear region are more reliable than those made in the saturation region. The noise behavior of *p*- and *n*-channel devices is compared and contrasted. While the noise magnitude in *n*-channel devices correlated well with oxide trapped charge, in *p*-channel devices the correlation was actually better with interface trapped charge.

VI.B Effects of Ionizing Radiation on the Noise Properties of DMOS Power Transistors

Effects of Ionizing Radiation on the Noise Properties of DMOS Power Transistors[†]

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Abstract

The $1/f$ noise properties of DMOS (double-diffused MOS) power transistors were examined as a function of total ionizing dose. The results indicate that radiation causes significant changes in the frequency dependence of the noise of the power MOSFETs studied. Before exposure to radiation, the noise power spectral density indicated a $1/f^\lambda$ relationship where λ ranged from approximately 0.5 to 1.0. As the total dose level increased, λ approached unity, while the magnitude of the noise increased proportionally with the radiation-induced charge density. In addition, noise measurements were performed after irradiation, while the devices were annealing under a ±12 V bias. It was found that, under the +12 V bias, λ increased and under the -12 V bias, λ decreased. Finally, no correlation was found between the pre-irradiation $1/f$ noise magnitude and the radiation hardness of these DMOS power transistors.

I. INTRODUCTION

Low frequency, or $1/f$, noise is a well-known phenomenon associated with MOSFETs. It has been reported by various authors that a relationship exists between the density of traps near the Si/SiO_2 interface and the $1/f$ noise measured in the device [1-5]. Several detailed models for $1/f$ noise in MOSFETs have been presented and can be classified as number-fluctuation models [2, 6], mobility-fluctuation models [7, 8], or combinations of the two [5]. Because of the relationship between trap densities and $1/f$ noise, the noise properties of MOSFETs have been proposed as a useful diagnostic tool for determining trap densities [5].

In an ionizing radiation environment, MOS performance degrades primarily due to the buildup of oxide-trapped and interface-trapped charge [9, 10]. Oxide-trapped charge contributes a bias-independent trapped positive charge, which results in a parallel shift in the i-v characteristics of a device. Interface-trapped charge results in a bias-dependent trapped charge, which tends to stretch out the i-v characteristics of a device. The dominant effect resulting from these charges is a shift in the threshold voltage and a degradation in the carrier mobility and small signal gain of the device. The effect of radiation exposure on the operating characteristics of power MOSFETs has been studied by a number of authors over the past few years [11-16].

Past experiments have shown that the increase in radiation-induced trap density is accompanied by a proportional increase in the amount of $1/f$ noise present in MOS transistors [17]. Meisenheimer and Fleetwood [18] found that the magnitude of the noise in N-channel integrated MOSFETs correlates with the amount of radiation-induced positive oxide-trapped charge present during irradiation and anneal, but noise magnitude did not correlate with the interface-trapped charge. A correlation between pre-irradiation $1/f$ noise and radiation hardness has also been reported [19], and it was found that the magnitude of the $1/f$ noise present in an MOS device is correlated with the radiation-induced hole-trapping efficiency of the oxide [20]. The physical reasons for that correlation have been attributed to the simple oxygen vacancy near the Si/SiO_2 interface known to be present in the SiO_2 before irradiation.

This paper explores in detail the noise properties of irradiated power MOSFETs. The variation of the noise magnitude and the slope of the noise-power spectral density are examined as functions of total dose.

II. MEASUREMENT TECHNIQUE

Experimental N-channel DMOS (double-diffused MOS) power transistors manufactured by Harris Semiconductor were exposed to ionizing radiation in Co-60 sources at dose rates of 100 rad(Si)/min and 6000 rad(Si)/min. A +9 V bias was applied to the gate of the MOSFETs during irradiation. The pre-irradiation and post-irradiation $1/f$ noise in the devices was measured using a

low-noise (PAR Model 113) preamplifier and a Hewlett-Packard 3582A spectrum analyzer or a HP 3561A spectrum analyzer.

The power DMOS transistor differs most significantly from the conventional MOS transistor in that its channel is non-uniformly doped and high currents are achieved by connecting thousands of DMOS cells together in parallel. The high current requirements of the power MOSFET in the linear region made $1/f$ noise measurements impractical and unstable for devices biased in the linear region of operation. Thus, in order to get more repeatable and stable noise measurements, all noise measurements were obtained while the device was biased in the saturation region with a constant $I_{DS} = 10$ mA and $V_{DS} = 5$ V. With this low current bias in the saturated regime, no heating of the transistor occurred during measurements. The primary difference between measurements made in the linear region of operation and those made in the saturation region is that the potential distribution along the channel is non-constant in saturation. This factor, combined with the non-uniform doping in the channel region of DMOS transistors, is an inherent difficulty in comparing $1/f$ noise measurements in power MOSFETs with previous results obtained from conventional MOS transistors. In addition, the noise was examined at temperatures ranging from 77 K to 350 K. The noise magnitude increased slightly with decreasing temperature, but devices which exhibited low noise at room temperature also exhibited low noise relative to other devices over the entire temperature range examined. This was also true for devices which exhibited high noise magnitude. Finally measurements were performed on multiple devices in two laboratories (University of Arizona and Naval Weapons Support Center) with similar results using two slightly different setups.

Figure 1 depicts the experimental setup used for the noise measurements. The resistance R_S was used to stabilize the DC operating characteristics of the device under test (DUT), while the capacitance C_S was chosen so that the source of the DUT was seen as an AC ground at the frequencies of interest (i.e., from 10 Hz to 256 Hz). Throughout all measurements, the drain to source current and the drain to source voltage were found to vary by less then two tenths of a percent. The noise of the amplifier circuit was an order of magnitude or more below the noise of the DUT. Thermal noise, or white noise, of these power
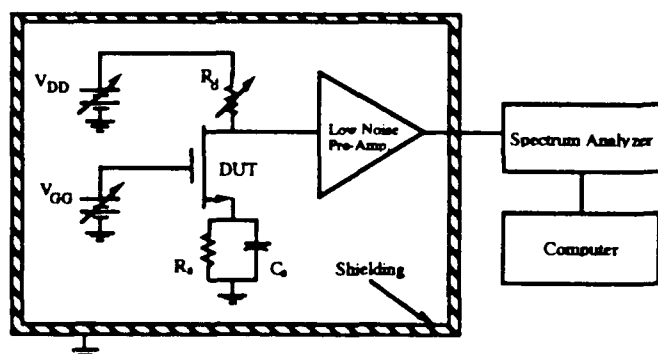
transistors was found to be insignificant compared to the $1/f$ noise measured, even to frequencies greater than 5 kHz. This was evidenced by approximate $1/f$ noise spectra well beyond the frequency range of interest. The equivalent noise-power spectral density seen at the gate of the MOS-FET is obtained from the small signal model of Figure 2:

$$S_{VG} = \frac{S_{VD}}{\left(g_m R_d\right)^2} \qquad (1)$$

where S_{VD} is the noise-power spectral density at the drain of the device, g_m is the transconductance of the device, and R_d is the resistance at the drain of the device.
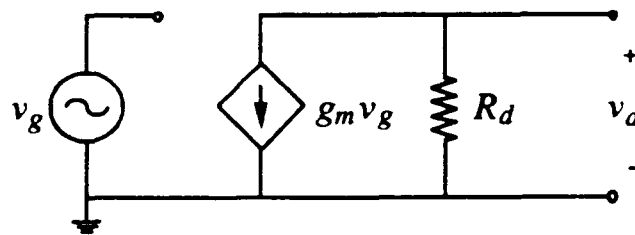
Fig. 2   Equivalent small signal circuit of a noise voltage source driving an MOS transistor.

The MOSFET subthreshold and threshold characteristic, as well as the transconductance, were obtained from an HP 4145B semiconductor parameter analyzer or a Reedholm RI-20 parameter analyzer. Post-irradiation voltage shifts were then obtained using the midgap extraction technique [21]. The radiation-induced noise was then compared to the radiation-induced voltage shifts, i.e., ΔV_{ot} and ΔV_{it}.

Noise measurements throughout the entire experiment were found to be very repeatable, using time averages of 256 measurements. The most sensitive part of the experiment is the measurement of the small signal gain of the transistor at its DC operating point, since this term becomes squared when calculating the equivalent noise power spectral density seen at the gate of the transistor. Figure 3 depicts the degradation in small signal gain, g_m, versus total dose. If this degradation in gain is not taken into account, then large errors in the equivalent noise will result.
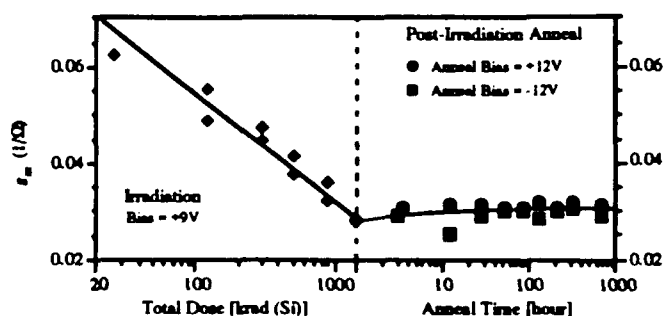
Fig. 1   Experimental setup used to measure the low frequency noise of an MOS transistor.

Fig. 3   Small signal gain, g_m, in the saturation region with a constant $I_{DS} = 10$ mA and $V_{DS} = 5$ V vs. total dose and total time annealing.

III. RESULTS

The square of the noise voltage for a typical device is plotted vs. frequency in Figure 4 with total ionizing radiation dose as a parameter. Before irradiation, the noise in a 1 Hz bandwidth was described by a noise-power spectral density of the form

$$S_{VG} = \frac{A}{f^{\lambda}} \qquad (2)$$

where, for the devices tested, λ ranged from approximately 0.5 to 1.0; and the noise magnitude A ranged from 10^{-14} to 10^{-12} V^2/Hz. After irradiation, λ increased and approached unity with increasing levels of total dose, as can be seen in Figure 5. During post-irradiation room-temperature (25°C) anneal, λ decreased under positive gate bias and λ increased under negative gate bias, as shown in Figure 6.

The magnitude of the noise spectrum and ΔV_{ot} are plotted vs. total dose and total time annealing in Figure 7, while Figure 8 depicts the variation in ΔV_{it}. The midgap method was used to estimate ΔV_{ot} and ΔV_{it} [21]. During irradiation, the magnitude of the $1/f$ noise increased
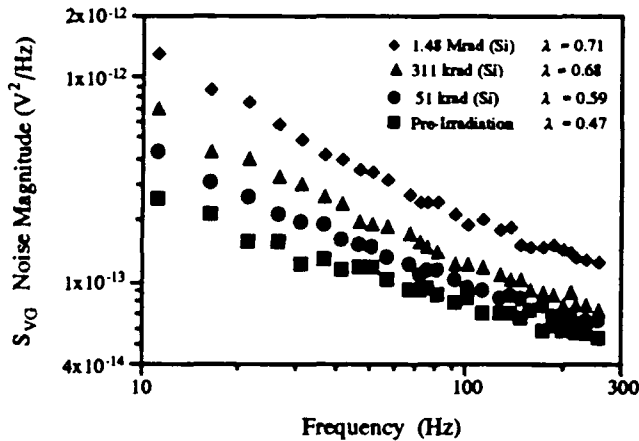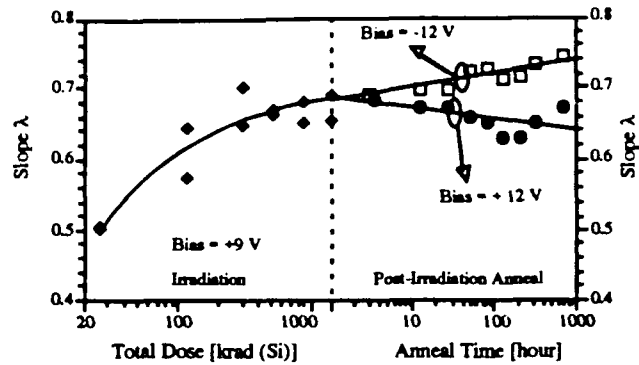

Fig. 6. Slope λ of noise measured vs. total dose and total time annealing.

approximately linearly with both radiation-induced voltage shifts ΔV_{it} and ΔV_{ot} (Shown in Fig. 9).

In Figures 7 and 8, the magnitude of the noise spectrum, $|\Delta V_{ot}|$, and ΔV_{it} increase with total dose. While annealing (Figure 7), the magnitudes of the $1/f$ noise and oxide-trapped charge decrease with time, while the interface-trapped charge increases (Figure 8) with time. Thus, the $1/f$ noise is more strongly correlated with the amount of oxide-trapped charge for devices positively biased than with the interface-trapped charge. This result is in agreement with previous results obtained by Meisenheimer and Fleetwood [18].

Figures 10 and 11 exhibit the $1/f$ noise characteristics for a device with positive bias applied during irradiation and negative bias applied during anneal. The oxide-

Fig. 4 Typical gate-voltage noise spectrum.

Fig. 7. $|\Delta V_{ot}|$ and noise magnitude vs. total dose and total time annealing for a typical device.
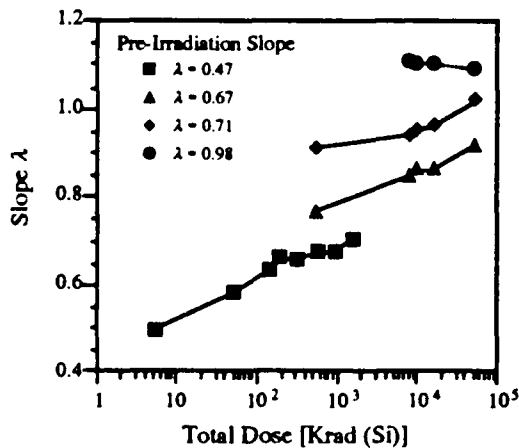
Fig. 5 Slope λ of noise vs. total dose for four different MOSFETs.
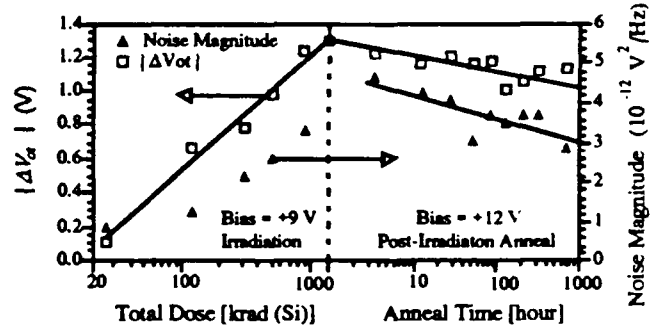

Fig. 8. ΔV_{it} and noise magnitude vs. total dose and total time annealing for a typical device.

Fig. 10 $|\Delta V_{ot}|$ and noise magnitude vs. total dose and total time annealing.

Fig. 11 ΔV_{it} and noise magnitude vs. total dose and total time annealing.

hardness reported in earlier work [19, 20] does not hold in these devices. This might be due to measurements performed in the saturated regime instead of the linear regime, and to the non-uniformly doped channel of the DMOS transistor. On the other hand, there appears to be a greater correlation with the slope λ and the radiation hardness of these power MOSFETs. It was found that devices with a slope λ between 0.60 and 0.70 tended to have little or no interface-trapped charge buildup, while devices with λ greater than 0.70 had a substantial buildup of interface-trapped charge, as evidenced by significant distortion of the post-irradiation subthreshold characteristics.
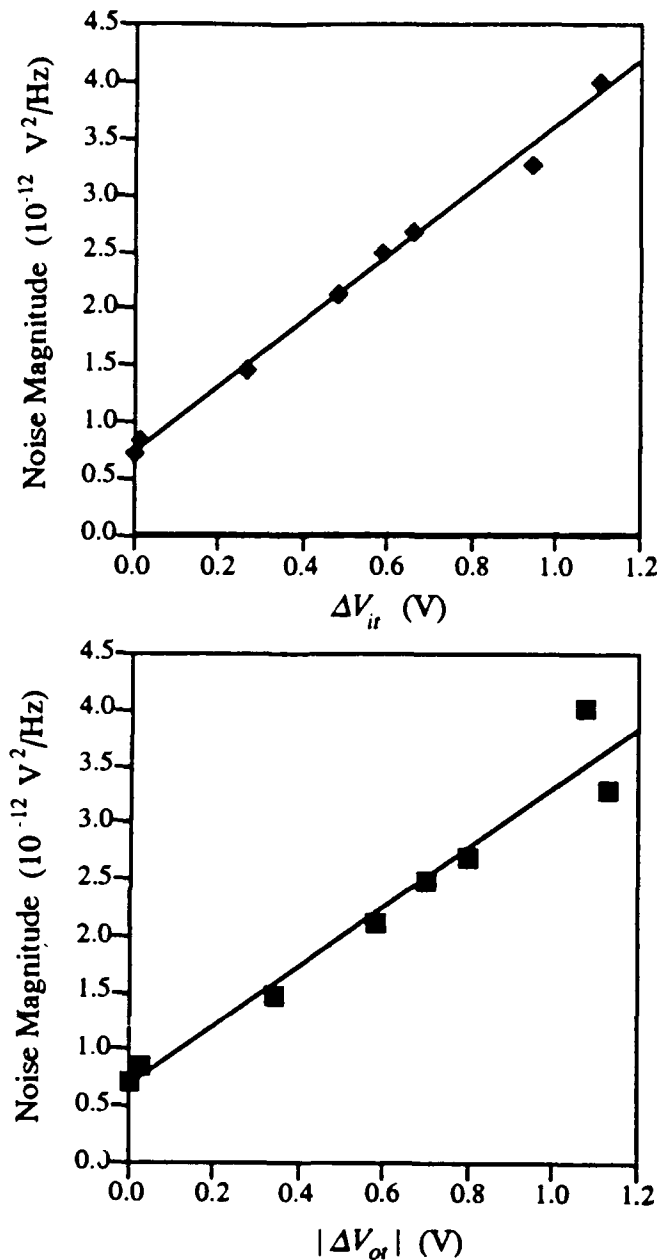

Fig. 9 Noise magnitude vs. ΔV_{it} and $|\Delta V_{ot}|$, measured pre-irradiation, and at dose levels of: 5 krad(Si), 51 krad(Si), 144 krad(Si), 188 krad(Si), 311 krad(Si), 882 krad(Si), and 1.48 Mrad(Si).

trapped charge and the interface-trapped charge increase slightly with anneal time, while the noise-magnitude data exhibit considerable scatter. Thus, these data do not allow conclusive determination of the relationship between noise magnitude and charge type for these bias conditions.

Figure 12 depicts the increase in $|\Delta V_{ot}|$ vs. total dose for three devices that were manufactured nominally the same, but were obtained from different lots. It can easily be seen that the characteristics of devices from lot 28 had the best radiation characteristics, while devices from lot 25 had the worst. However, devices from lot 25 had the lowest pre-rad noise magnitude. This indicates that the relationship between pre-rad noise magnitude and radiation
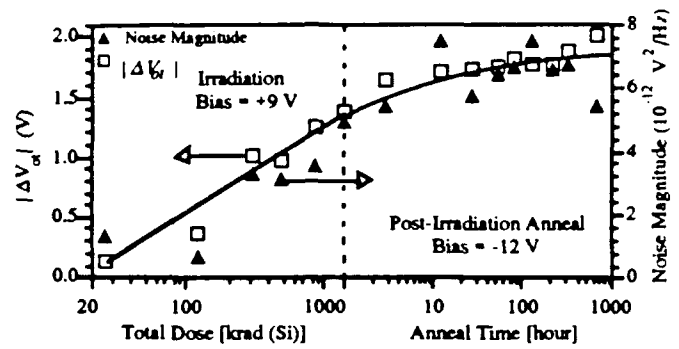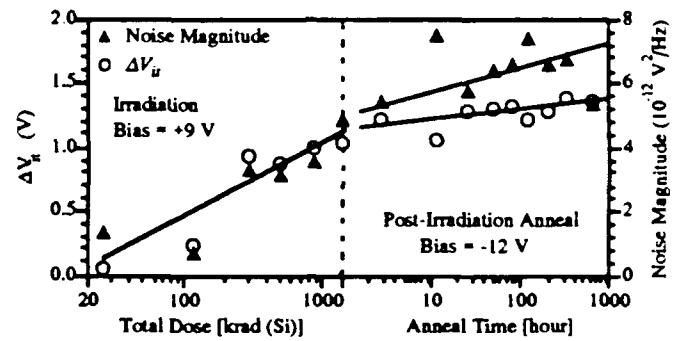
IV. DISCUSSION AND CONCLUSIONS

The fluctuation of the charge carriers in the channel due to their interaction with traps located within the oxide is one of the dominant factors responsible for the $1/f^{\lambda}$ noise behavior [2]. If the distribution of the traps in the oxide leads to a distribution of time constants that is skewed towards the higher frequency range, then λ is less than unity [2, 4]. If, after gamma-radiation, the distribution of time constants becomes more uniform, then λ approaches unity. This trend is noted in Figure 4. During anneal, a +12 V bias initially reduced the slope of the noise, while a -12 V bias forced the slope to further increase towards unity. Thus, the bias field applied during anneal may have forced a change in the charge or trap distribution near the Si/SiO$_2$ interface that the $1/f$ noise was sensitive to.

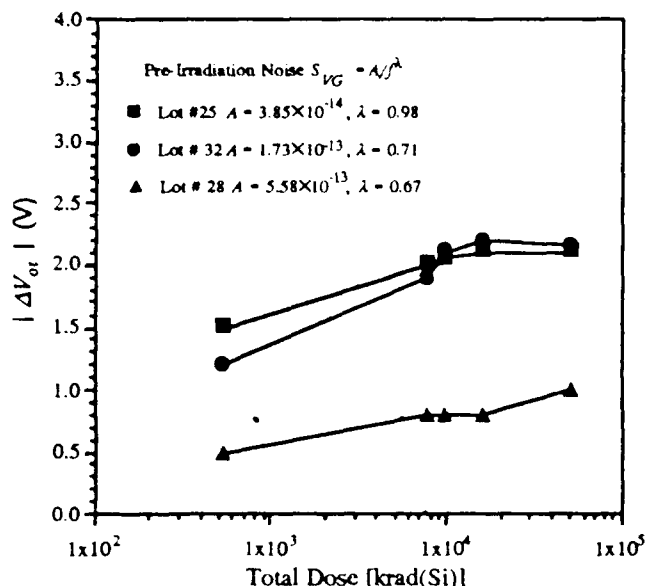All of the devices tested exhibited increasing noise

Fig. 12 $|\Delta V_{ot}|$ vs. total dose for three nominally identical devices with different pre-irradiation noise levels.

magnitude with increasing total dose levels. However, no correlation seemed to exist between their pre-rad noise magnitude and radiation hardness. This lack of correlation may be due to the non-uniform channel-region doping and measuring the noise in the saturated region of operation, unlike earlier work in which such a correlation was observed [19]. Data displayed in Figure 5 clearly indicate that ionizing radiation tends to produce a more uniform distribution in the time constants associated with the low-frequency noise in DMOS devices. Finally, the lot with the lowest slope λ, but the highest initial noise magnitude, exhibited the least sensitivity to radiation. These results suggest that additional studies of the relationship between λ and the interface-trapping mechanisms in MOS transistors may be productive. This, in turn, could lead to the use of low-frequency noise measurements as a nondestructive technique for determining the radiation hardness of MOS devices.

Acknowledgment

The authors would like to express their sincere thanks to Benjamin Senitzky for enlightening discussions. The continued interest of LCDR Lewis Cohn and Dale Platteter is appreciated. Finally, the authors wish to thank Dan Fleetwood and Timothy Meisenheimer of Sandia National Laboratories for valuable discussions on measurement technique and $1/f$ noise.

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VI.C Comparison of $1/f$ Noise in Irradiated Power MOSFETs Measured in the Linear and Saturation Regions

Comparison of 1/f noise in irradiated power MOSFETs measured in the linear and saturation regions

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Abstract

1/f noise in n-channel and p-channel power MOSFETs is investigated as a function of total dose and annealing. A different evolution of the noise measured in the linear and saturation regions is reported.

I-Introduction

1/f noise measurements on MOSFETs have been reported for a long time. 1/f noise is related to defects located at the Si/SiO_2 interface or in the oxide close to the interface [1-3]. Time constants describing the exchange of carriers between these traps and the channel depend on the location of these defects. The use of 1/f noise measurements as a characterization tool for irradiated devices stems from the various kinetics involved in the build-up of defects during irradiation and anneal, which results in different behaviors of noise magnitude as a function of the total dose and annealing time [4-7].

Most 1/f noise measurements previously reported were done on integrated-circuit MOSFETs biased in the linear region [4-7]. Only saturation-regime noise measurements have been reported in power MOSFETs [8]. Measurements in power MOSFETs operated in the linear regime involve the following problems specific to the the structure of power devices:

(1)   A power MOSFET contains thousands of identical cells operated in parallel which act as uncorrelated sources of noise. Thus, a power MOSFET is equivalent to a conventional lateral transistor with a very large gate area. As the noise level is inversely proportional to the gate area, the overall noise level of these devices is far below the noise associated with integrated-circuit MOSFETs.

(2)   The magnitude of the static drain current needed to properly bias the transistor in the linear region is drastically increased in comparison to that required in integrated-circuit MOSFETs. This necessitates an improved power supply and a reduction in value of the drain load resistor. This leads to heating problems in peripheral components and eventually in the device under test itself. The possibility of further instabilities and inaccuracies of noise measurements is therefore increased.

These problems are not so critical if noise measurements are taken when the transistor is biased in the saturation region. In that case, the static drain current can be reduced as the noise level increases by one or two orders of magnitude. The goal of this paper is to evaluate the reliability of noise measurements in the saturation regime as compared to those performed in the linear regime. The 1/f noise measurements in the linear regime have been proposed as a characterization tool for radiation-induced defects in integrated-circuit MOSFETs [4-7]. In this paper, the feasibility of linear-regime noise measurements in power MOSFETs is demonstrated for the first time.

II-Experimental results and discussion

The devices used in this study were non-hardened IRF440 n-channel power MOSFETs and MTM8P08 p-channel power MOSFETs manufactured by Motorola. The irradiations were performed in a Co^{60} source up to a total dose of 10 krad(Si). The dose rate was 500 rad(Si)/hour. During both the radiation exposure and a subsequent anneal, the gates of the transistors were biased at + 9 V, while the sources and drains were grounded.

The biasing conditions used for the 1/f noise measurements are given in Table 1. These values were kept constant for all measurements through irradiation and annealing. The choice of bias conditions in the linear regime is critical for proper device characterization. The transistor must be biased so that pre-radiation noise levels are significantly above the background noise level. On the other hand, the drain current must be kept low in order to avoid heating effects. The choice of bias conditions in the saturation regime is not as critical, and the range of acceptable values is wider.

	IRF440	MTM8P08
Linear regime	V_G-V_T = 0.5 V V_{DS} = 0.1 V	V_G-V_T = - 0.5 V V_{DS}= - 0.1 V
Saturation regime	V_G-V_T = 0.2 V V_{DS} = 5 V	V_G-V_T = - 0.2 V V_{DS} = - 5 V

Table 1. Bias conditions during 1/f measurements.

The non-uniform doping along the channel of power MOSFETs results in different values of the surface potential along the channel for a given gate voltage. Even though this may be expected to adversely affect the applicability of models used for noise in integrated-circuit MOSFETs, we found that the pre-irradiation noise for n-channel and p-channel transistors is well described by [3-7] :

$$S_{Vd} = \frac{K}{f^\alpha} \frac{V_{DS}^2}{(V_G - V_T)^2} \tag{1}$$

Note that in power MOSFETs, the value of the drain-to-source voltage V_{DS} must be modified by taking the effect of non-negligible drain series resistance into account. Namely, with a drain current close to 100 mA during the noise measurement, the voltage drop across that parasitic resistance can be of the order of the voltage actually applied across the channel.

Pre-irradiation noise measured in the saturation region is for these devices an increasing function of (V_G - V_T) and it is independent of V_{DS} .

$$S_{Vd} = \frac{K'}{f^\alpha} (V_G - V_T)^\beta \qquad 2 \le \beta \le 3 \tag{2}$$

All the noise measurements were taken in the frequency range from 1 to 250 Hz. For frequencies higher than 100 Hz, the noise becomes close to the background noise for power MOSFETs biased in the linear regime. Only frequencies between 2 and 100 Hz were used for fitting the data to Eqns. 1 and 2.

The increase in the noise magnitude as a function of the total dose is illustrated in Figs. 1 and 2. In both n-channel and p-channel transistors, the noise measured in the linear region increases by more than one order of magnitude after a total dose of 10 krad(Si). However, the noise measured in the saturation region remains almost unchanged up to the total dose of 10 krad(Si).

The midgap charge separation technique was used to determine the contributions of oxide-trapped charge (ΔV_{ot}) and interface-trapped charge (ΔV_{it}) to the threshold voltage shift (ΔV_T) [9]. A correlation between noise measured in the linear or saturation regime and ΔV_{ot} and ΔV_{it} was investigated for both n-channel and p-channel power MOSFETs. The noise measured in the linear region correlates with ΔV_{ot} (and not ΔV_{it}) for the n-channel devices through irradiation and anneal. However, for the p-channel devices, the noise continues to increase during annealing despite a decrease in ΔV_{ot}, indicating better correlation with ΔV_{it}. The change in the noise measured in saturation was much less pronounced for both n-channel and p-channel devices. Figures 3 and 4 plot the noise vs. ΔV_{ot} for the n-channel devices and noise vs. ΔV_{it} for the p-channel devices through both irradiation and anneal, respectively.

The noise slope (α in Eqns. 1 and 2) of all the parts was not significantly affected by irradiation and subsequent anneal and remained in the range from 0.85 to 1.09.

III-Conclusions

The noise behavior of both n-channel and p-channel power transistors is investigated. Noise measurements on power devices biased in the linear regime are reported for the first time. A proper choice of bias conditions is essential for applicability of linear-regime 1/f noise measurements in these devices, in light of problems specific to power MOSFETs biased in the linear regime.

Pre-irradiation noise and its evolution through irradiation and anneal are found to be in agreement with previously published results for integrated-circuit MOSFETs biased in the linear region [4-7]. Furthermore, the build-up of interface traps was found to correlate well with the increase of noise during annealing for the p-channel devices.

Measurements taken in the saturation regime do not correlate as well with radiation-induced charge build-up, even though the overall noise increases slightly during irradiation.

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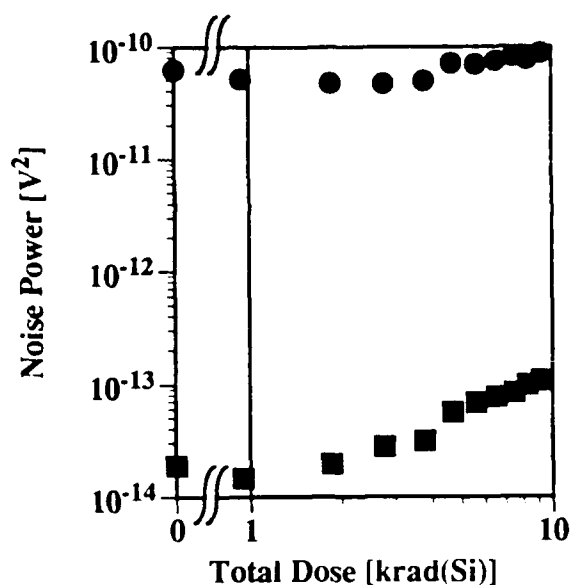
Fig. 1- Noise power as a function of the total dose for an n-channel power MOSFET. Noise was measured in the linear region (squares) and .n the saturation region (circles).

Fig. 2- Noise power as a function of the total dose for a p-channel power MOSFET. Noise was measured in the linear region (squares) and in the saturation region (circles).

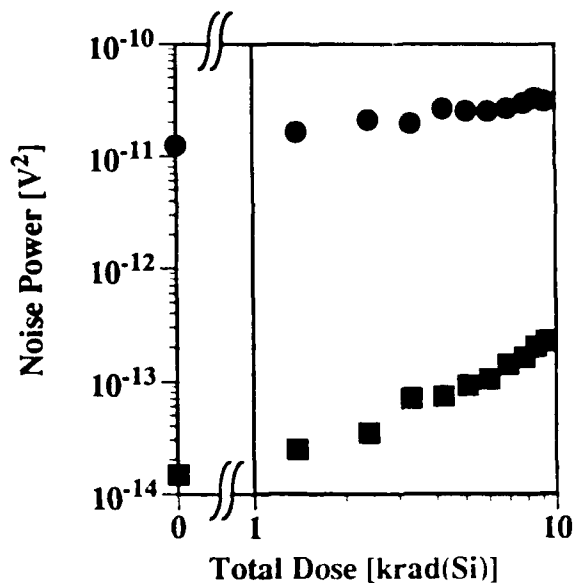**Fig. 3-** Noise power as a function of ΔV_{ot} of an n-channel power MOSFET during irradiation and annealing. Noise was measured in the linear region (squares) and in the saturation region (circles).
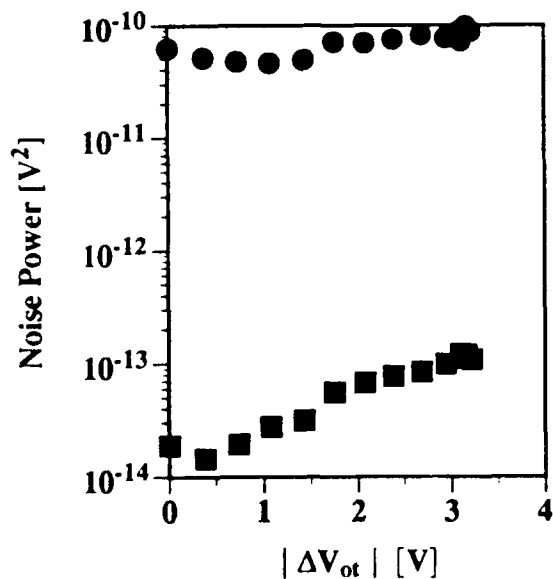
Fig. 4- Noise power as a function of ΔV_{it} for a p-channel power MOSFET during irradiation and annealing. Noise was measured in the linear region (squares) and in the saturation region (circles).
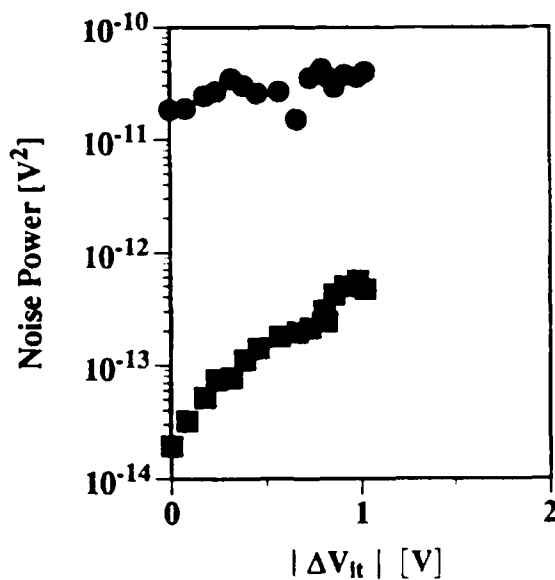
VII. Summary and Conclusions

This report has covered work on modeling of single event burnout of power MOSFETs, single event burnout of power bipolar transistors, simulation of the effect of ionizing radiation on power-MOSFET breakdown voltage, charge buildup in field oxides, and $1/f$ noise in power MOSFETs. Each technical section of this report is self-contained.

Each technical section describes work that has contributed to the technical base necessary to provide radiation-hardened power MOSFETs for DNA-supported systems. Much of the work has yielded design guidelines that can be used in the development of radiation-hardened power MOSFETs. This work has been widely disseminated through technical talks and technical papers, and through direct consultation with government laboratory personnel and personnel from the power-device industry.

VIII. Acknowledgment

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